dresden elektronik

User Manual
Radio Modules

deRFsam3-13M10
deRFsam3-23M10-2
deRFsam3-23M10-3R

Document Version V1.1
2014-04-22

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Document history

Date	Version	Description
2013-07-02	1.0	Initial version
2014-04-22	1.1	Update external components for deRFsam3-23M10-3R Update maximum output power register setting section Addition of fiducial marker description

Abbreviations

Abbreviation	Description
IEEE 802.15.4	Communication standard, applicable to low-rate Wireless Personal Area Networks (WPAN)
6LoWPAN	IPv6 over Low Power Wireless Personal Area Networks
ADC	Analog to Digital Converter
EMI	Electromagnetic Interference
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
GPIO	Generals Purpose Input Output
JTAG	Joint Test Action Group, digital interface for debugging of embedded devices, also known as IEEE 1149.1 standard interface
ISA SP100	International Society of Automation, the Committee establishes standards and related technical information for implementing wireless systems.
ISP	In-System-Programming
LGA	Land Grid Array, a type of surface-mount packaging for integrated circuits
LNA	Low Noise Amplifier
MAC	Medium (Media) Access Control
MCU, µC	Microcontroller Unit
PA	Power Amplifier
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RF	Radio Frequency
R&TTE	Radio and Telecommunications Terminal Equipment (Directive of the European Union)
SPI	Serial Peripheral Interface
TWI	Two Wire Interface

1. Overview

The tiny radio module series by dresden elektronik combines Atmel's 32-bit ARM Cortex-M3 ATSAM3S4 with a small footprint. Three different module types are available, depending on the custom application. The form factors are all identical.

The deRFsam3-13M10 has the onboard sub-GHz transceiver AT86RF212 which supports the frequency ranges of 868.3 MHz for EU and 902 to 928 MHz for US. The deRFsam3-23M10-2 has the onboard 2.4 GHz low-cost transceiver AT86RF232 which supports the frequency range of 2.45 GHz for worldwide applications. The deRFsam3-23M10-3R has the onboard 2.4 GHz transceiver AT86RF233 which supports the frequency range of 2.45 GHz for worldwide applications.

The customer is free to design it's own antenna, coaxial output or front end but it is also possible to use one of dresden elektronik's certified and documented RF designs. Provided adapter boards make the tiny modules pin- and mechanically compatible with dresden elektronik evaluation modules.

2. Application

The main applications for the radio modules are:

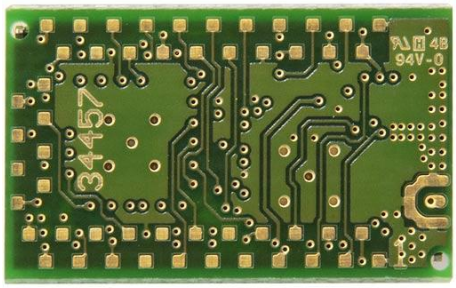
- 2.4 GHz and sub-GHz IEEE 802.15.4
- ZigBee® Pro
- ZigBee RF4CE
- ZigBee IP
- 6LoWPAN
- ISA SP100
- Wireless Sensor Networks (WSN)
- Industrial and home controlling and monitoring
- Smart Metering

3. Features

3.1. deRFsam3-13M10

The radio module deRFsam3-13M10 offers the following features:

- Tiny size: 21.5 x 13.2 x 3.0 mm
- 55 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Usable signals: power supply, peripheral, programming, debugging, tracing, ADC, GPIO
- Onboard 18.432 MHz crystal (MCU clock) and 16 MHz crystal (Transceiver clock with +/- 10 ppm frequency deviation)



- Application interfaces:
  1 x USB, 3 x UART, 2 x TWI, 1x ADC
- Debug/Programming interfaces:
  1 x JTAG
- Solderable sub-GHz RF output pads (1x RFOUT, 3x RFGND)
- Certification: CE, FCC pending

Figure 1 shows the block diagram of the radio module deRFsam3-13M10.

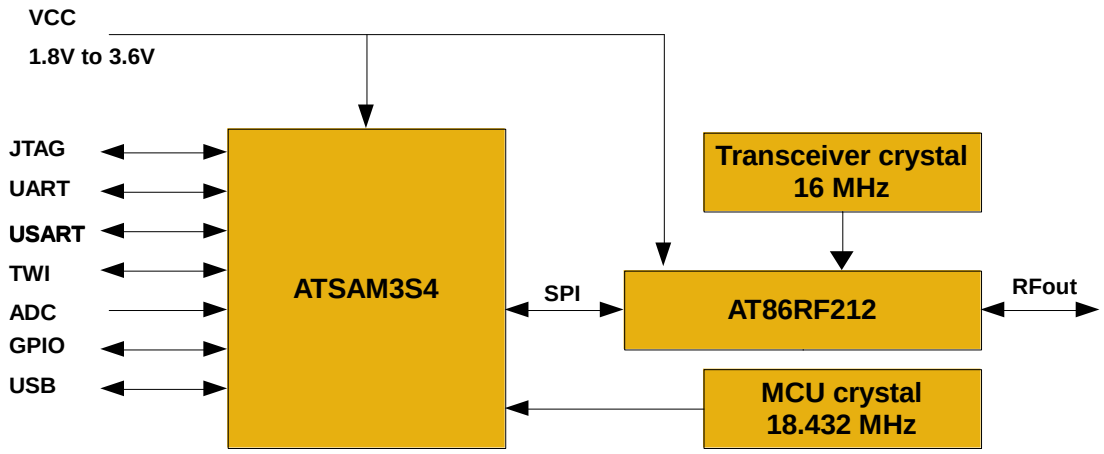
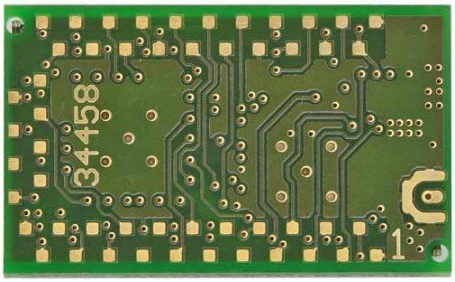


Figure 1: block diagram deRFsam3-13M10

3.2. deRFsam3-23M10-2

The radio module deRFsam3-23M10-2 offers the following features:

- Tiny size: 21.5 x 13.2 x 3.0 mm
- 55 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Usable signals: power supply, peripheral, programming, debugging, tracing, ADC, GPIO
- Onboard 18.432 MHz crystal (MCU clock) and 16 MHz crystal (Transceiver clock with +/- 10 ppm frequency deviation)



- Application interfaces:
  1 x USB, 3 x UART, 2 x TWI, 1x ADC
- Debug/Programming interfaces:
  1 x JTAG
- Solderable sub-GHz RF output pads (1x RFOUT, 3x RFGND)
- Certification: CE, FCC pending

Figure 2 shows the block diagram of the radio module deRFsam3-23M10-2.

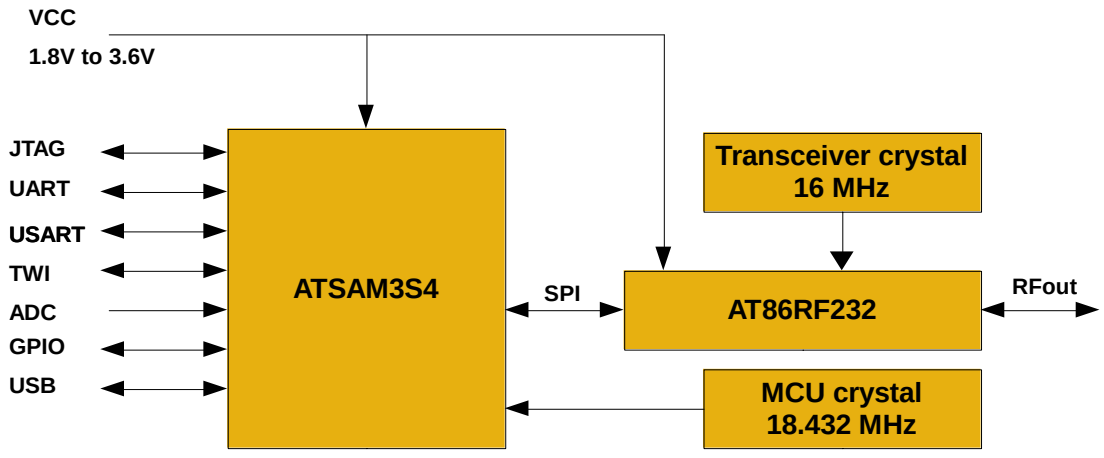
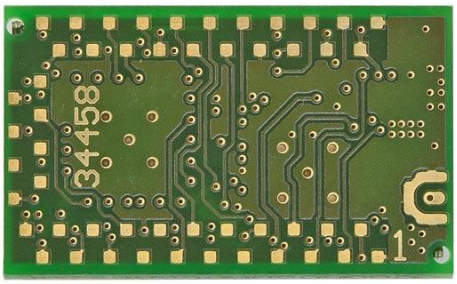


Figure 2: block diagram deRFsam3-23M10-2

3.3. deRFsam3-23M10-3R

The radio module deRFsam3-23M10-3R offers the following features:

- Tiny size: 21.5 x 13.2 x 3.0 mm
- 55 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Usable signals: power supply, peripheral, programming, debugging, tracing, ADC, GPIO
- Onboard 18.432 MHz crystal (MCU clock) and 16 MHz crystal (Transceiver clock with +/- 10 ppm frequency deviation)



- Application interfaces:
  1 x USB, 3 x UART, 2 x TWI, 1x ADC
- Debug/Programming interfaces:
  1 x JTAG
- Solderable sub-GHz RF output pads (1x RFOUT, 3x RFGND)
- Certification: CE, FCC pending

Figure 3 shows the block diagram of the radio module deRFsam3-23M10-3R.

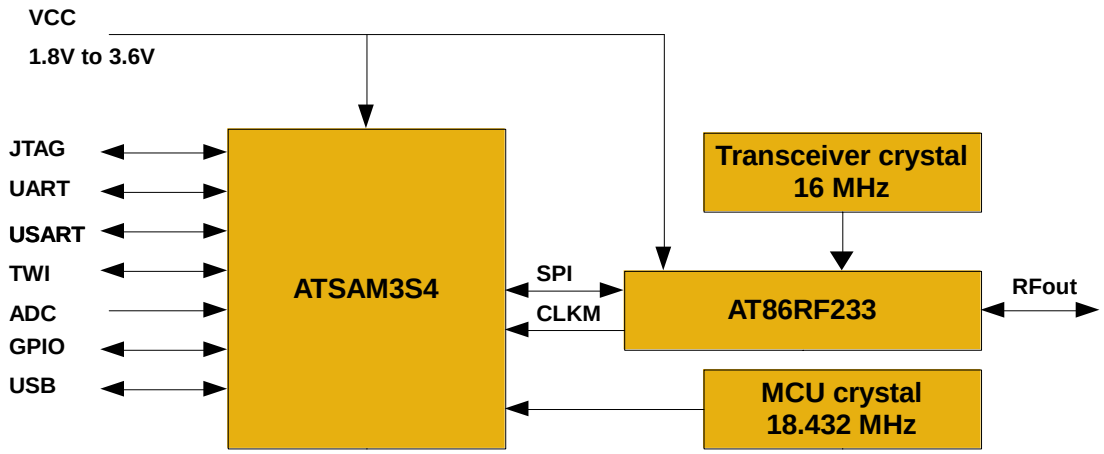


Figure 3: block diagram deRFsam3-23M10-3R

4. Technical data

Table 1: Mechanical data

Mechanical	
Radio modules	
Size (L x W x H)	21.5 x 13.2 x 3.0 mm
Pads	
Type	LGA
Pitch	1.60 mm
Pad size	0.6 x 0.6 mm

Table 2: Temperature range

Temperature range					
		Min	*Typ*	*Max*	*Unit*
Operating temperature range	T_{work}	-40		+85	°C
Humidity		25		80	% r.H.
Storage temperature range	$T_{storage}$	-40		+125	°C

Table 3: Electrical data

Electrical[1]					
deRFsam3-13M10					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply voltage	VCC	1.8	3.3	3.6	V
Current consumption (US mode)	I_{TXon} (TX_PWR = +10 dBm)	48.4	53.7	53.8	mA
	I_{TXon} (TX_PWR = +5 dBm)	46.4	50.7	50.8	mA
	I_{TXon} (TX_PWR = +3 dBm)	42.1	44.7	44.8	mA
	I_{Txon} (TX_PWR = 0 dBm)	40.3	42.7	42.8	mA
	I_{Txon} (TX_PWR = -11 dBm)	37.5	39.6	39.7	mA
	I_{Rxon}	35.3	37.2	37.3	mA
	I_{Sleep} (depends on sleep mode)	TBD	TBD	TBD	µA
deRFsam3-23M10-2					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply voltage	VCC	1.8	3.3	3.6	V

[1] All current values measured at MCU clock of 32.000 MHz

Current consumption	I_{TXon} (TX_PWR = +3 dBm)	40.0	42.1	42.2	mA
	I_{TXon} (TX_PWR = +0 dBm)	38.6	40.4	40.5	mA
	I_{TXon} (TX_PWR = -17 dBm)	34.5	35.8	35.9	mA
	I_{RXon}	38.3	40.0	40.1	mA
	I_{Sleep} (depends on Sleep Mode)	TBD	TBD	TBD	µA
deRFsam3-23M10-3R					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply voltage	VCC	1.8	3.3	3.6	V
Current consumption	I_{TXon} (TX_PWR = +4 dBm)	38.5	40.9	41.0	mA
	I_{TXon} (TX_PWR = +0 dBm)	37.1	39.2	39.3	mA
	I_{TXon} (TX_PWR = -17 dBm)	33.5	35.2	35.3	mA
	I_{RXon}	37.7	39.7	39.8	mA
	I_{Sleep} (depends on Sleep Mode)	TBD	TBD	TBD	µA

Table 4: Quartz crystal properties

Quartz crystal					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
MCU crystal	Frequency		18.432		MHz
	Frequency tolerance		+/- 30		ppm
Transceiver crystal	Frequency		16.000		MHz
	Frequency tolerance		+/-10		ppm

Table 5: Radio data of deRFsam3-13M10

Radio 2.4GHz (Supply voltage VCC = 3.3V)					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
RF pad	Impedance		50		Ω
	Diversity		No		
Range	line of sight		TBD		m
Frequency range	PHY_CC_CCA = 0x00		868.3		MHz
	PHY_CC_CCA = 0x01…0x0A	906		924	MHz
Channels	PHY_CC_CCA = 0x00		1		
	PHY_CC_CCA = 0x01…0x0A		10		

Transmitting power (conducted) [2]	TX_PWR = 0xE1	6.6	8.3	8.4	dBm
	TX_PWR = 0x62	3.7	3.9	4.0	dBm
Receiver sensitivity (conducted)	Data Rate = 20 kBit/s Data Rate = 100 kBit/s Data Rate = 200 kBit/s Data Rate = 400 kBit/s		-104 -97 -94 -89		dBm dBm dBm dBm
	Data Rate = 40 kBit/s Data Rate = 250 kBit/s Data Rate = 500 kBit/s Data Rate = 1000 kBit/s		-102 -97 -95 -91		dBm dBm dBm dBm
Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x08 TRX_CTRL_2 = 0x09 TRX_CTRL_2 = 0x2A		20 100 200 400		kBit/s kBit/s kBit/s kBit/s
	TRX_CTRL_2 = 0x04 TRX_CTRL_2 = 0x0C TRX_CTRL_2 = 0x0D TRX_CTRL_2 = 0x2E		40 250 500 1000		kBit/s kBit/s kBit/s kBit/s

Table 6: Radio data of deRFsam3-23M10-2

Radio (Supply voltage VCC = 3.3V)					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
RF pad	Impedance		50		Ω
	Diversity		No		
Range			TBD		m
Frequency range		2405		2480	MHz
Channels			16		
Transmitting power conducted		3.2	3.6	3.7	dBm
Receiver sensitivity	Data Rate = 250kBit/s		-99		dBm
Data rate (gross)	TRX_CTRL_2 = 0x00		250		kBit/s

[2] Measured without external low-pass filter

Table 7: Radio data of deRFsam3-23M10-3R

Radio (Supply voltage VCC = 3.3V)					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
RF pad	Impedance		50		Ω
	Diversity		No		
Range			TBD		m
Frequency range		2405		2480	MHz
Channels			16		
Transmitting power conducted		2.2	2.6	2.7	dBm
Receiver sensitivity	Data Rate = 250kBit/s Data Rate = 500kBit/s Data Rate = 1000kBit/s Data Rate = 2000kBit/s		-98 -95 -93 -87		dBm dBm dBm dBm
Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x01 TRX_CTRL_2 = 0x02 TRX_CTRL_2 = 0x03		250 500 1000 2000		kBit/s kBit/s kBit/s kBit/s

4.1. Necessary external components for deRFsam3-13M10

The sub-GHz radio module deRFsam3-13M10 needs external RF filter components to decrease spurious emissions and to fulfill the requirements of FCC Part 15 Subpart C § 15.209. Possible solutions are discrete or integrated low-pass filters. We recommended a discrete Pi-type low-pass filter pictured in **Figure 4**. The filter network results in a slightly higher current consumption in transmit and receive mode of about 1 mA and a decreased output power of 1 dB. Integrated filters may have better performance values. Place the filter directly next to the radio module RF pad trace to ensure a proper function. The used parts are listed in **Table 8**. Of course it is allowed to use equivalent parts of other manufacturers with similar or equal properties.

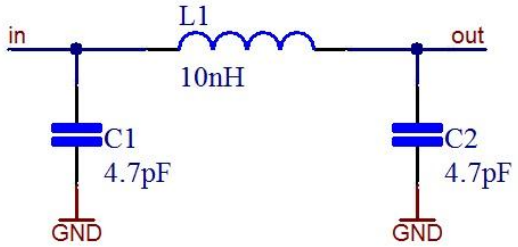


Figure 4: Schematic low-pass filter

Table 8: BOM discrete low-pass filter

Part	Value	Package	Manufacturer	Type
C1	4.7 pF	0402	Yageo	CC0402CRNP09BN4R7
L1	10 nH	0402	Taiyo Yuden	HK100510NJ-T
C2	4.7 pF	0402	Yageo	CC0402CRNP09BN4R7

4.2. Necessary external components for deRFsam3-23M10-3R

The 2.4 GHz radio module deRFsam3-23M10-3R needs external RF filter components to decrease spurious emissions and to fulfill the requirements of FCC Part 15 Subpart C § 15.209. Possible solutions are discrete or integrated low-pass filters. We recommended a discrete low-pass filter like shown in **Figure 5**. The filter network causes an output power decrease of 1 dB. Integrated filters may have better performance values. Place the filter directly next to the radio module RF pad to ensure a proper function. The recommended parts are listed in **Table 9**. Of course it is possible to use equivalent parts of other manufacturers with similar or equal properties.

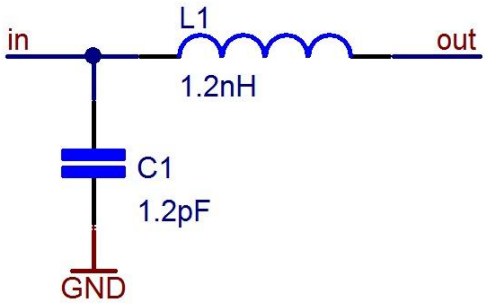


Figure 5: Schematic low-pass filter

Table 9: BOM discrete low-pass filter

Part	Value	Package	Manufacturer	Type
C1	1.2pF	0402	Yageo	CC0402CRNP09BN1R2
L1	1.2nH	0402	Taiyo Yuden	HK10051N2J-T

4.3. Maximum output power settings

Table 10, **Table 11** and **Table 12** show the maximum allowed power register setting for each available channel.

Table 10: EU power table for deRFsam3-13M10

Region	ETSI [EU mode]	
Data rate	BPSK20,	OQPSK100, OQPSK200, OQPSK400
Channel	TX_PWR [hex]	TX_PWR [hex]
0	0x63	0x64

Table 11: FCC power table for deRFsam3-13M10

Region	FCC [US mode]	
Data rate	BPSK20	OQPSK250, OQPSK500, OQPSK1000
Channel	TX_PWR [hex]	TX_PWR [hex]
1	0x00	0xE1
2	0x00	0xE1
3	0x00	0xE1
4	0x00	0xE1
5	0x00	0xE1
6	0x00	0xE1
7	0x00	0xE1
8	0x00	0xE1
9	0x00	0xE1
10	0x00	0xE1

Table 12: FCC and EU power table for deRFsam3-23M10-2 and deRFsam3-23M10-3R

Region	EU [ETSI]	US [FCC]
Data rate	OQPSK250, OQPSK500, OQPSK1000, OQPSK2000	
Channel	TX_PWR [hex]	TX_PWR [hex]
11	0x00	0x00
12	0x00	0x00
13	0x00	0x00
14	0x00	0x00
15	0x00	0x00
16	0x00	0x00
17	0x00	0x00
18	0x00	0x00
19	0x00	0x00
20	0x00	0x00
21	0x00	0x00
22	0x00	0x00
23	0x00	0x00
24	0x00	0x00
25	0x00	0x00
26	0x00	0x0A

4.4. TX power register settings for deRFsam3-13M10

Table 13 shows the current consumption and conducted output power during transmission depending on the **recommended** TX_PWR register setting. The deRFsam3-13M10 features the EU and US region modes.

Table 13: Recommended TX_PWR register settings

Region	EU [ETSI]	US [FCC]	
Data rate	BPSK20, OQPSK100, OQPSK200, OQPSK400	BPSK40	OQPSK250, OQPSK500, OQPSK1000
TX Power [dBm]	TX_PWR [hex]	TX_PWR [hex]	TX_PWR [hex]
10			0xE1
9			0xA1
8			0x81
7			0x82
6		0x00	0x83
5		0x02	0x84
4	0x62	0x03	0x85
3	0x63	0x04	0x42
2	0x64	0x05	0x22
1	0x65	0x07	0x23
0	0x66	0x24	0x24
-1	0x47	0x25	0x25
-2	0x48	0x04	0x04
-3	0x28	0x05	0x05
-4	0x29	0x06	0x06
-5	0x2A	0x07	0x07
-6	0x08	0x08	0x08
-7	0x09	0x09	0x09
-8	0x0A	0x0A	0x0A
-9	0x0B	0x0B	0x0B
-10	0x0C	0x0C	0x0C
-11	0x0D	0x0D	0x0D

4.4.1. Setting for US mode with data rate BPSK40

Figure 6 and **Figure 7** show the current consumption and conducted output power during transmission depending on the US mode TX_PWR register setting of deRFsam3-13M10. The diagrams are valid for the data rate BPSK40.

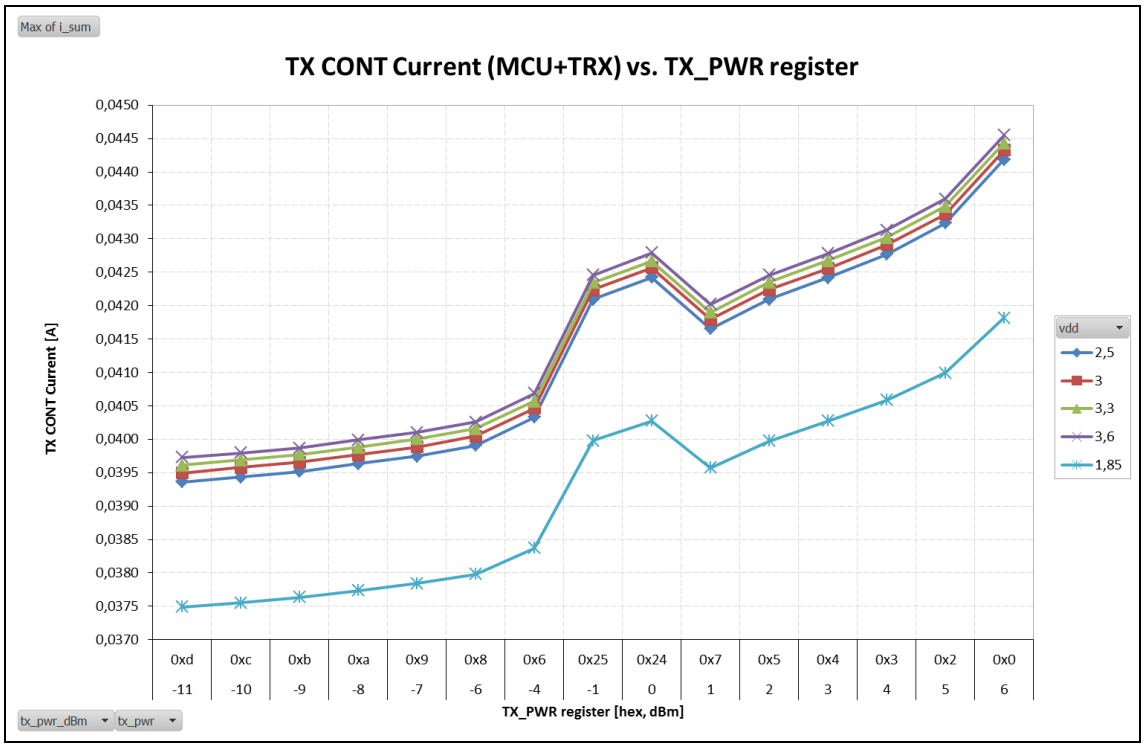


Figure 6: US BPSK40 mode TX Idd vs. TX_PWR for deRFsam3-13M10

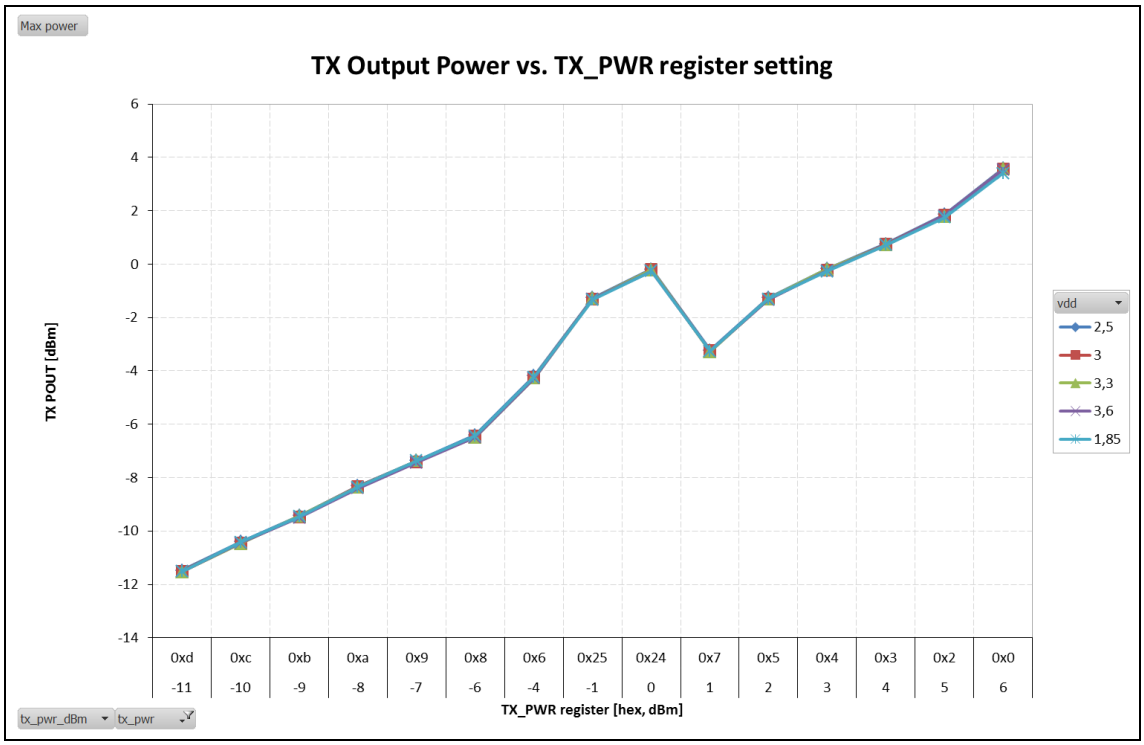


Figure 7: US BPSK40 mode TX Pout vs. TX_PWR for deRFsam3-13M10

4.4.2. Setting for US mode with data rate OQPSK250/500/1000

Figure 8 and **Figure 9** show the current consumption and conducted output power during transmission depending on the US mode TX_PWR register setting of deRFsam3-13M10. The diagrams are valid for the data rates OQPSK250/500/1000.

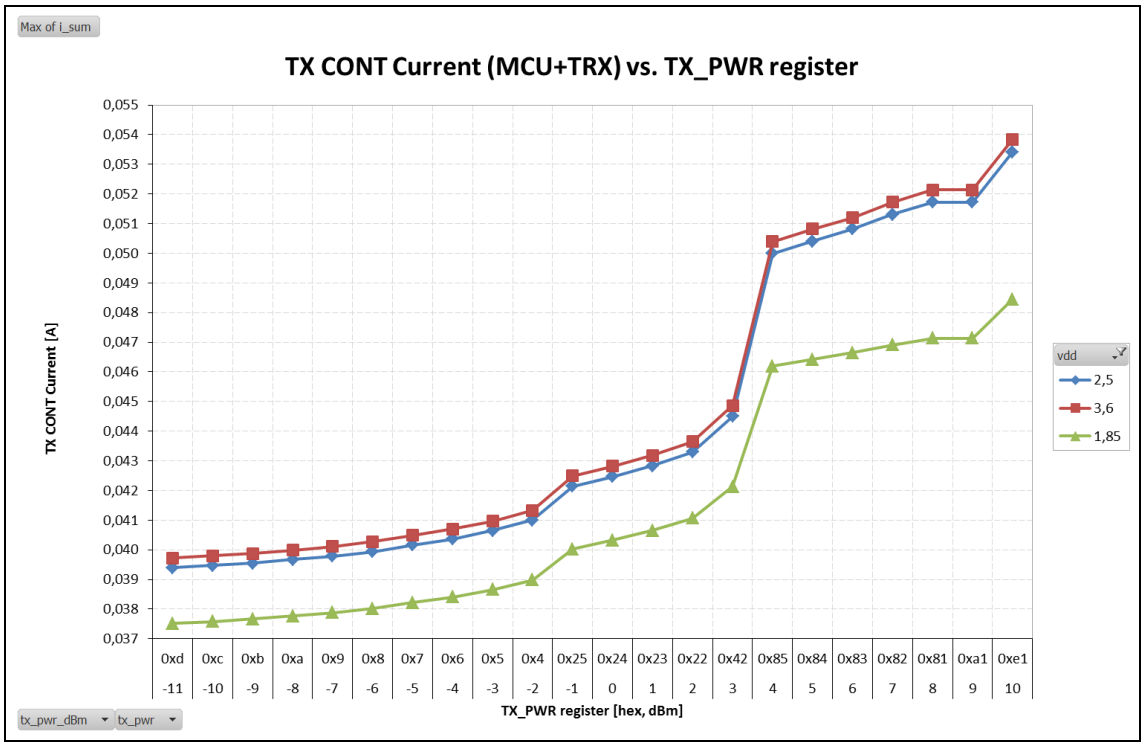


Figure 8: US OQPSK mode TX Idd vs. TX_PWR for deRFsam3-13M10

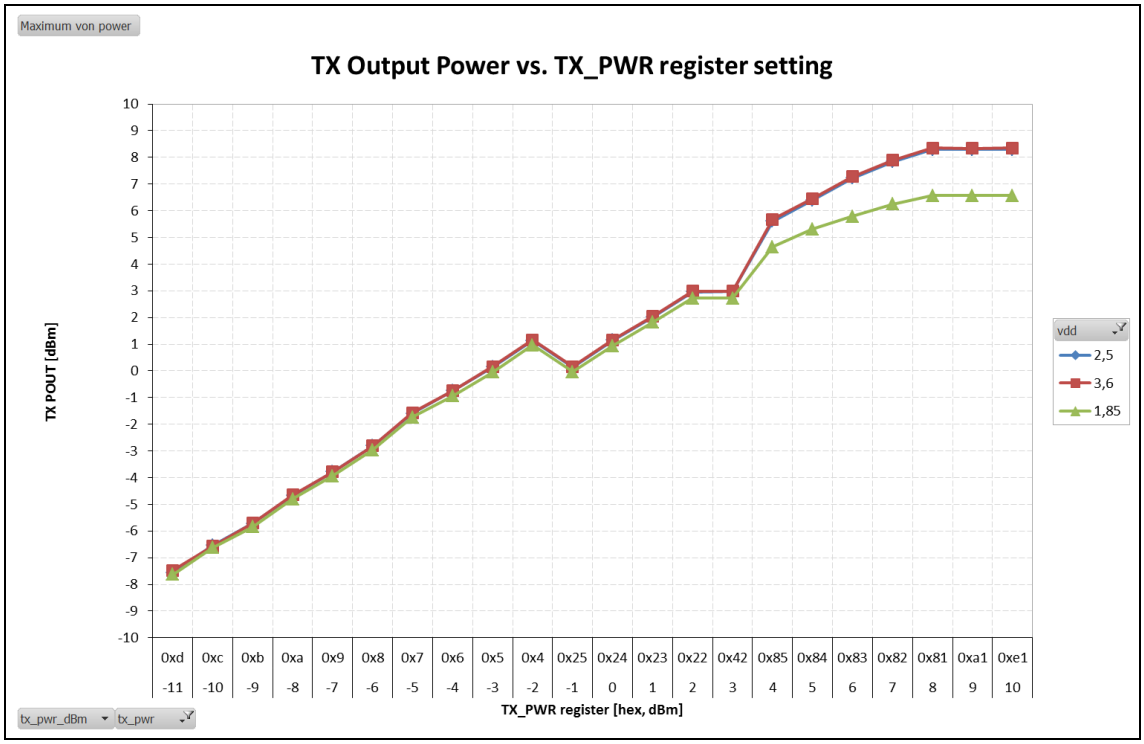


Figure 9: US OQPSK mode TX Pout vs. TX_PWR for deRFsam3-13M10

4.4.3. Setting for EU mode

Figure 10 and **Figure 11** show the current consumption and conducted output power during transmission depending on the EU mode TX_PWR register setting of deRFsam3-13M10.

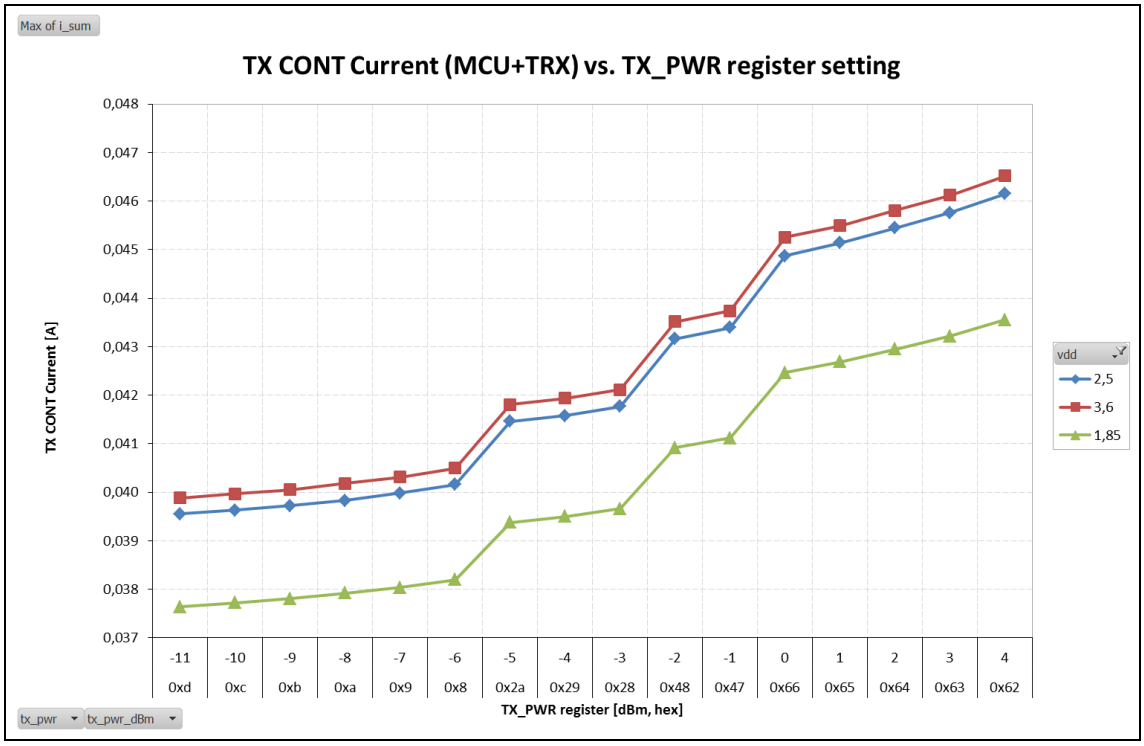


Figure 10: EU TX Idd vs. TX_PWR for deRFsam3-13M10

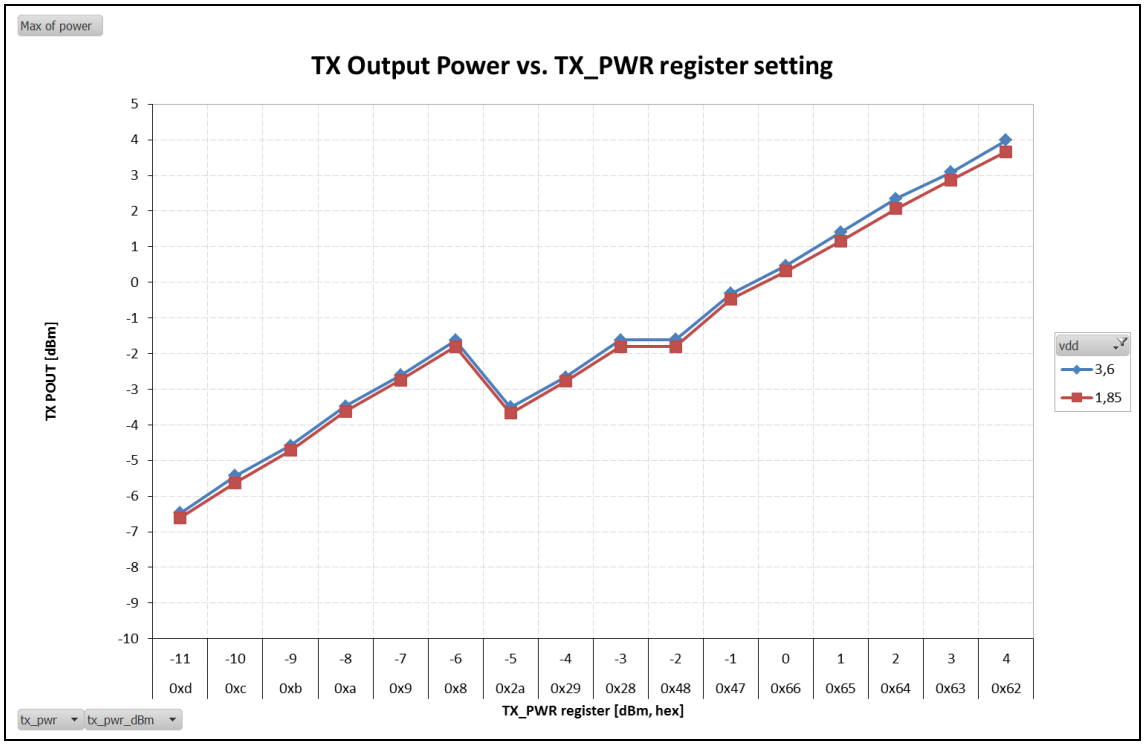


Figure 11: EU TX Pout vs. TX_PWR for deRFsam3-13M10

4.5. TX power register settings for deRFsam3-23M10-2

Figure 12 and **Figure 13** show the current consumption and conducted output power during transmission depending on the TX_PWR register setting of deRFsam3-23M10-2.

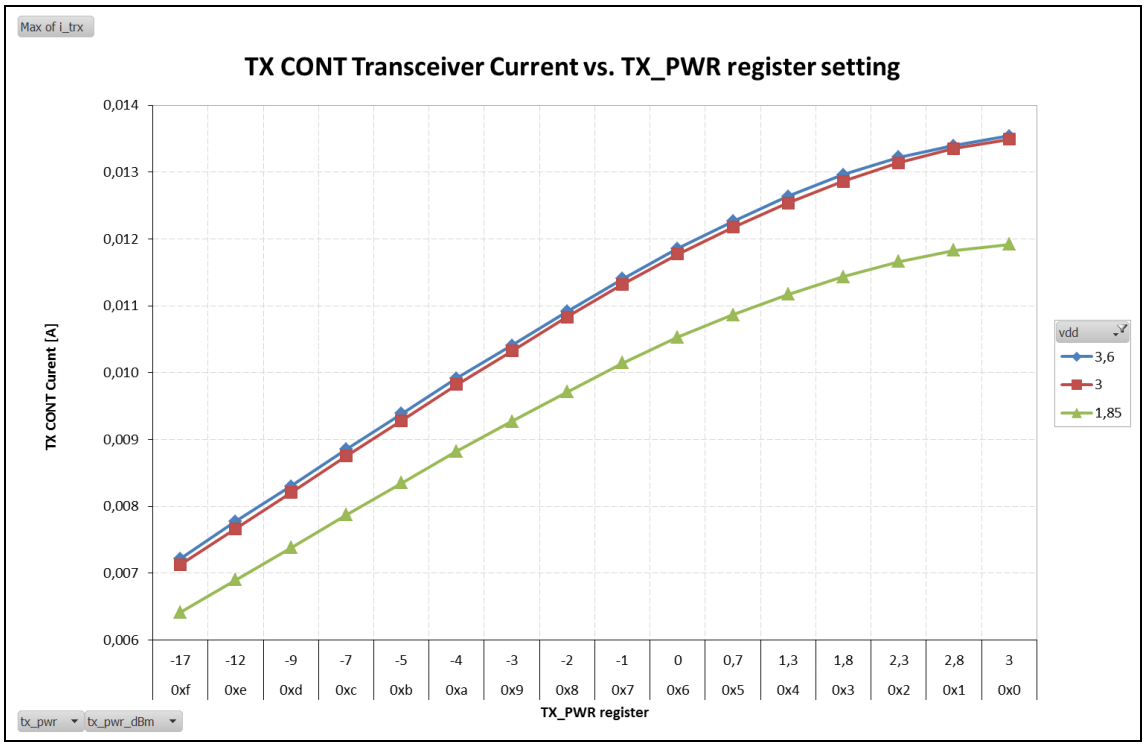


Figure 12: TX Idd vs. TX_PWR for deRFsam3-23M10-2

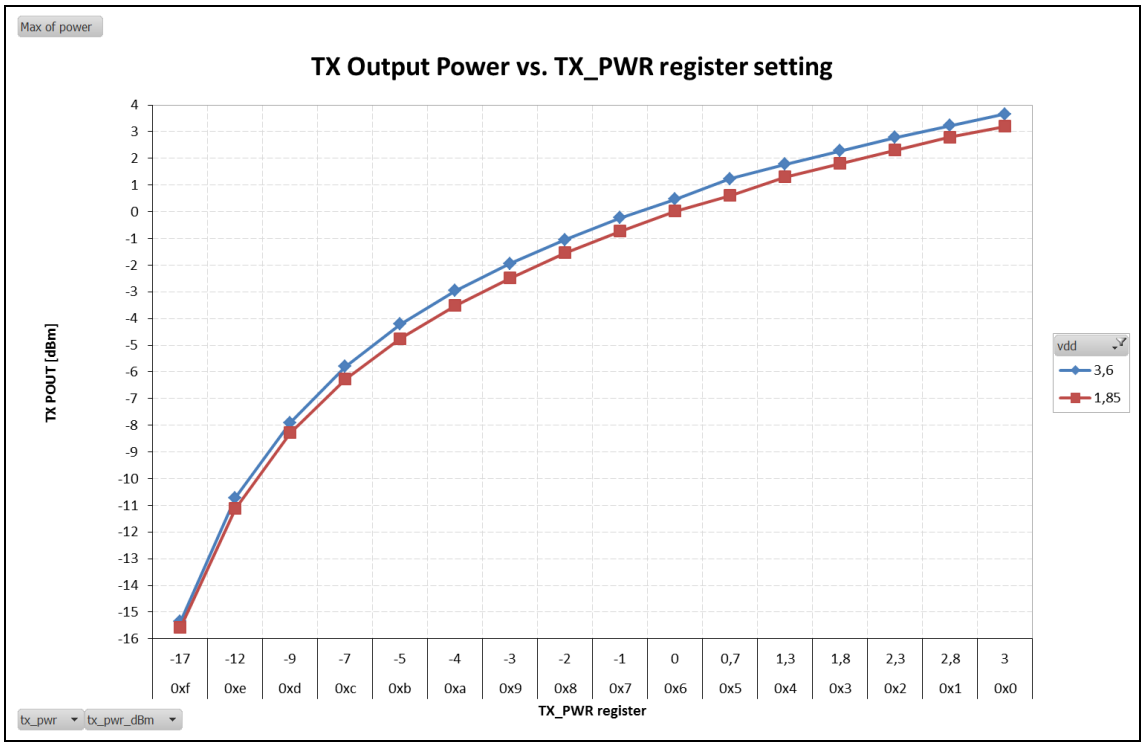


Figure 13: TX Pout vs. TX_PWR for deRFsam3-23M10-2

4.6. TX power register settings for deRFsam3-23M10-3R

Figure 14 and **Figure 15** show the current consumption and conducted output power during transmission depending on the TX_PWR register setting of deRFsam3-23M10-3R.

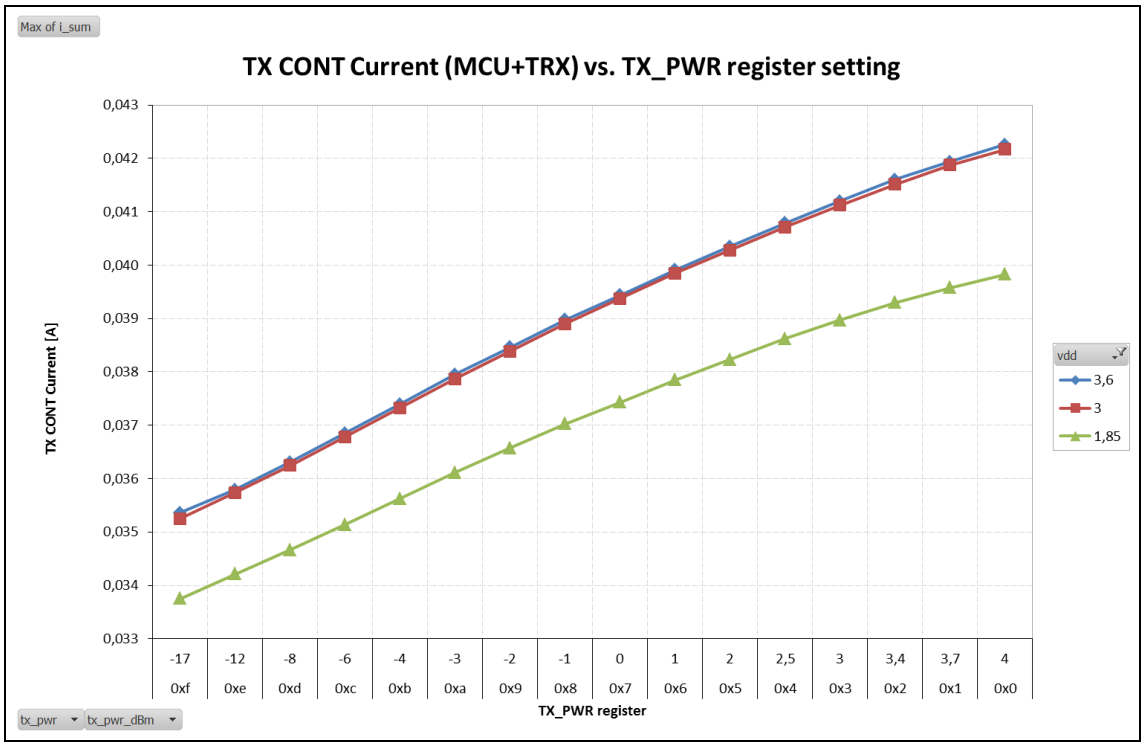


Figure 14: TX Idd vs. TX_PWR for deRFsam3-23M10-3R

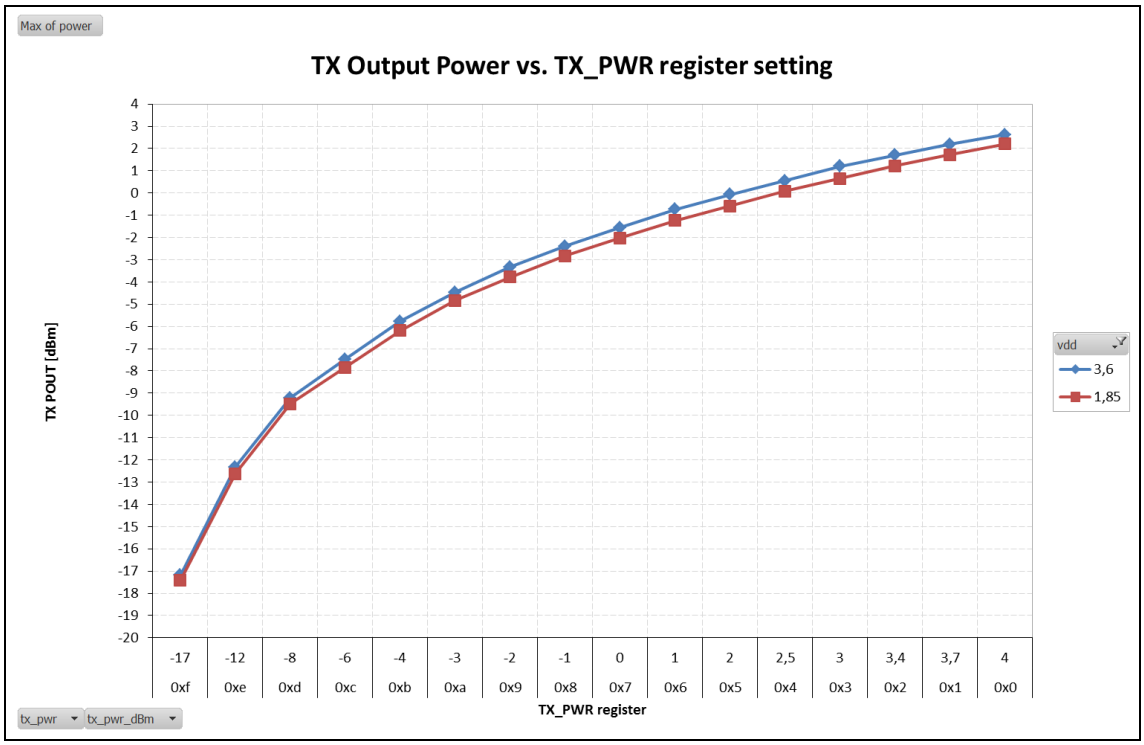


Figure 15: TX Pout vs. TX_PWR for deRFsam3-23M10-3R

5. Mechanical size

The following section show the mechanical dimensions of the different radio modules. All distances are given in millimeters.

5.1. Size of deRFsam3-13M10, 23M10-2 and 23M10-3R

The module has a size of 21.5 x 13.2 mm and a height of 3.0 mm. The LGA pads are arranged in a double row design. **Figure 16** shows the details from top view.

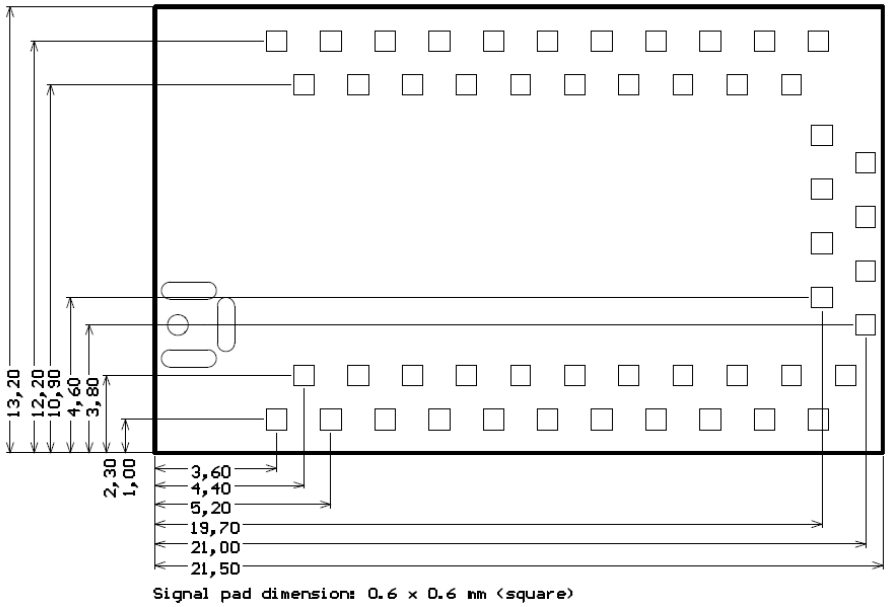


Figure 16: Size of module and signal pads (top view)

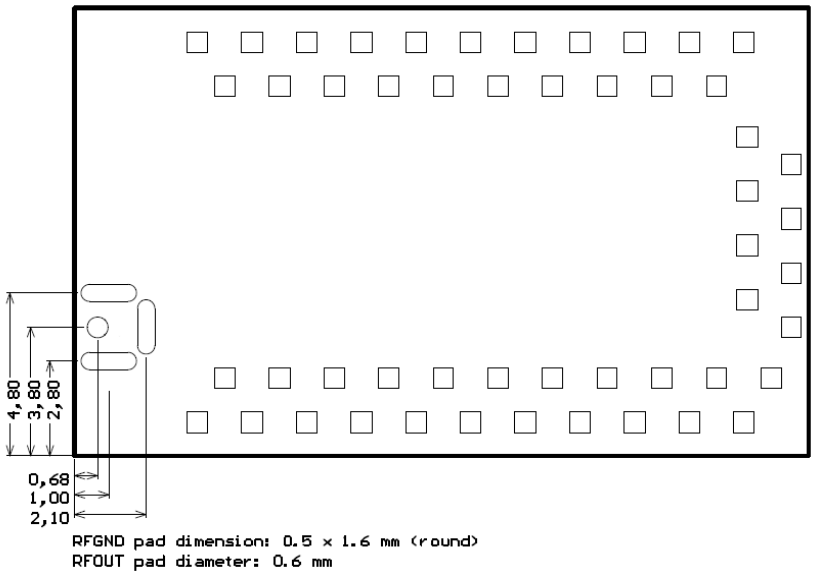


Figure 17: Size of RF pads (top view)

6. Soldering profile

Table 14 shows the recommended soldering profile for the radio modules.

Table 14: Soldering Profile

Profile Feature	Values
Average-Ramp-up Rate (217°C to Peak)	3°C/sec. max.
Preheat Temperature 175°C ±25°C	180 sec. max
Temperature Maintained Above 217°C	60 sec. to 150 sec.
Time within 5°C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260°
Ramp-down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 min. max.

Figure 18 shows a recorded soldering profile for a radio module. The blue colored line illustrates a temperature sensor placed next to the soldering contacts of the radio module. The pink line shows the set temperatures depending on the zone within the reflow soldering machine.

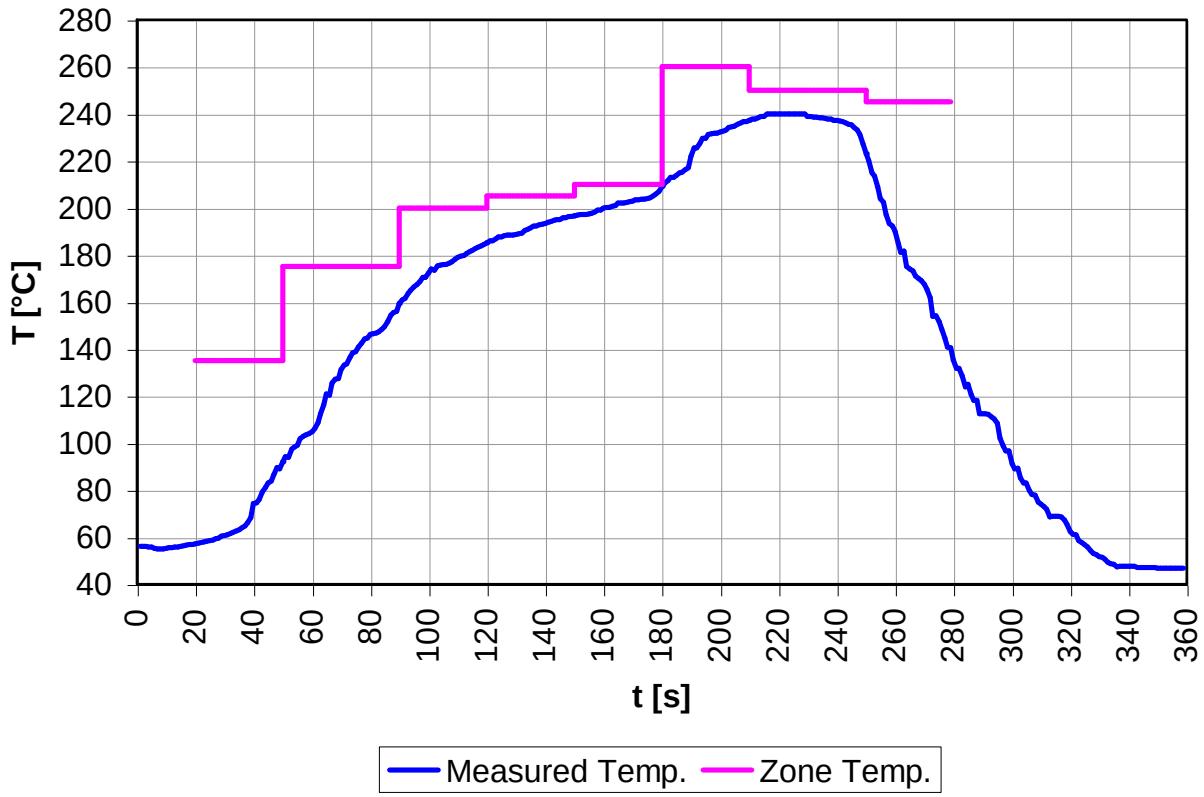


Figure 18: Recorded soldering profile

A solder process without supply of nitrogen causes a discoloration of the metal RF shielding. It is possible that the placed label shrinks due the reflow process.

7. Pin assignment

The LGA pads provide the all signals to the customer: power supply, peripheral, programming, debugging, tracing, analog measurement, external front-end control, antenna diversity control and free programmable ports. All provided signals except VCC, DGND, RSTN, JTAGSEL, TST, AREF and AVDD are free programmable port pins (GPIO).

7.1. Signals of deRFsam3-13M10

The radio module deRFsam3-13M10 has 55 LGA pads. The '1' marking is shown in **Figure 20**. Consider that the pin numbering in **Figure 21** is shown from top view. All available LGA pads are listed in **Table 15**.

Figure 19: deRFsam3-13M10 (top view)

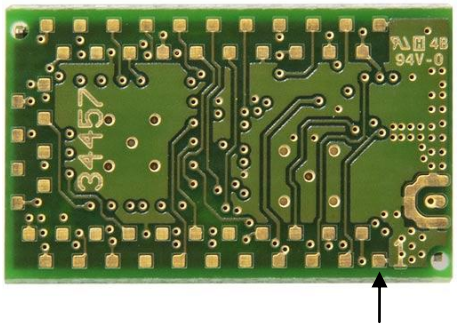


Figure 20: deRFsam3-13M10 (bottom view)

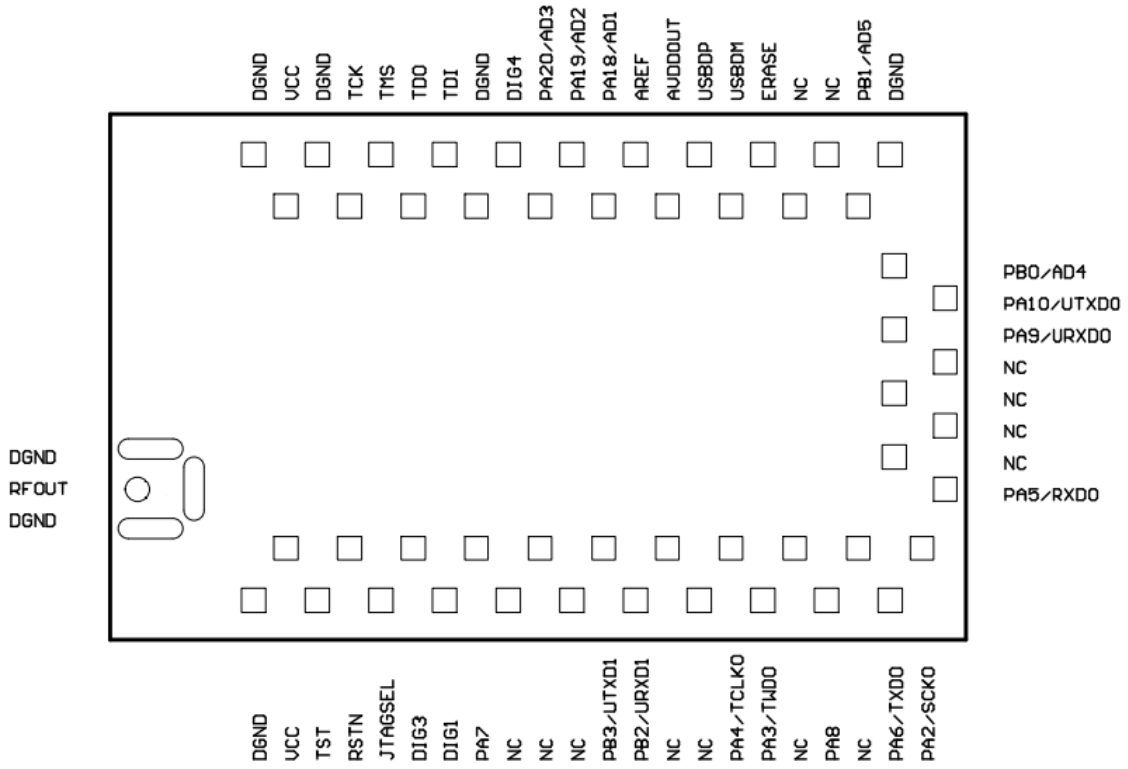


Figure 21: Pad numbering and signal names of deRFsam3-13M10 (top view)

Table 15: Description of available LGA pads and I/O port pins for deRFsam3-13M10

Description of available I/O port pins on header pins							
LGA Pad	*MCU Pin*	*TRX Pin*	*I/O port pin*	*Alternate function (signal name)*			*Comments*
1	-	-	GND				
2	-	-	VCC				1.8 V to 3.6 V
3	30	-	TST				**Must be connected to GND!**
4	29	-	RSTN				Reset
5	38	-	JTAGSEL				Leave unconnected if unused
6	-	1	DIG3				Transceiver output pin
7	-	9	DIG1				Transceiver output pin
8	24	-	PA7	RTS0	PWMH3	XIN32	
9	-	-	NC				Leave unconnected
10	-	-	NC				Leave unconnected
11	-	-	NC				Leave unconnected
12	6	-	PB3	UTXD1	PCK2	AD7	UART1
13	5	-	PB2	URXD1	NPCS2	AD6	UART1
14	-	-	NC				Leave unconnected
15	-	-	NC				Leave unconnected
16	28	-	PA4	TWCK0	TCLK0		TWI
17	31	-	PA3	TWD0	NPCS3		TWI
18	-	-	NC				Leave unconnected
19	23	-	PA8	CTS0		XOUT32	
20	-	-	NC				Leave unconnected
21	26	-	PA6	TXD0	PCK0		USART0
22	32	-	PA2	SCK0	PWMH2		USART0
23	27	-	PA5	RXD0	NPCS3		USART0
24	-	-	NC				Leave unconnected
25	-	-	NC				Leave unconnected
26	-	-	NC				Leave unconnected
27	-	-	NC				Leave unconnected
28	22	-	PA9	URXD0	NPCS1	PWMFI0	UART0
29	21	-	PA10	UTXD0	NPCS2		UART0
30	3	-	PB0		PWMH0	AD4	
31	-	-	GND				

32	4	-	PB1		PWM1	AD5	
33	-	-	NC				Leave unconnected
34	-	-	NC				Leave unconnected
35	42	-	PB12		PWML1	ERASE[3]	ERASE pin depending on program method necessary
36	43	-	PB10	DDM			Native USB
37	44	-	PB11	DDP			Native USB
38	29	-	AVDDOUT				**Leave unconnected if unused (1.8 V TRX Voltage Output)** Internal 1 uF capacitor
39	1	-	AREF				No internal capacitor assembled
40	10	-	PA18		PCK2	AD1	
41	11	-	PA19		PWML0	AD2	
42	12	-	PA20		PWML1	AD3	
43	-	2	DIG4				Transceiver output pin
44	-	-	GND				
45	25	-	PB4	TWD1	PWMH2	TDI	JTAG
46	37	-	PB5	TWCK1	PWML0	TDO	JTAG
47	39	-	PB6	SWDIO		TMS	JTAG
48	40	-	PB7	SWCLK		TCK	JTAG
49	-	-	GND				
50	-	-	VCC				1.8 V to 3.6 V
51	-	-	GND				

[3] See **Section** Fehler! Verweisquelle konnte nicht gefunden werden. for more information of the usage of ERASE pin

7.2. Signals of deRFsam3-23M10-2

The radio module deRFsam3-23M10-2 has 55 LGA pads. The '1' marking is shown in **Figure 23**. Consider that the pin numbering in **Figure 24** is shown from top view. All available LGA pads are listed in **Table 16**.

Figure 22: deRFsam3-23M10-2 (top view)

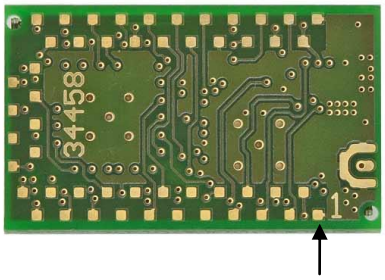


Figure 23: deRFsam3-23M10-2 (bottom view)

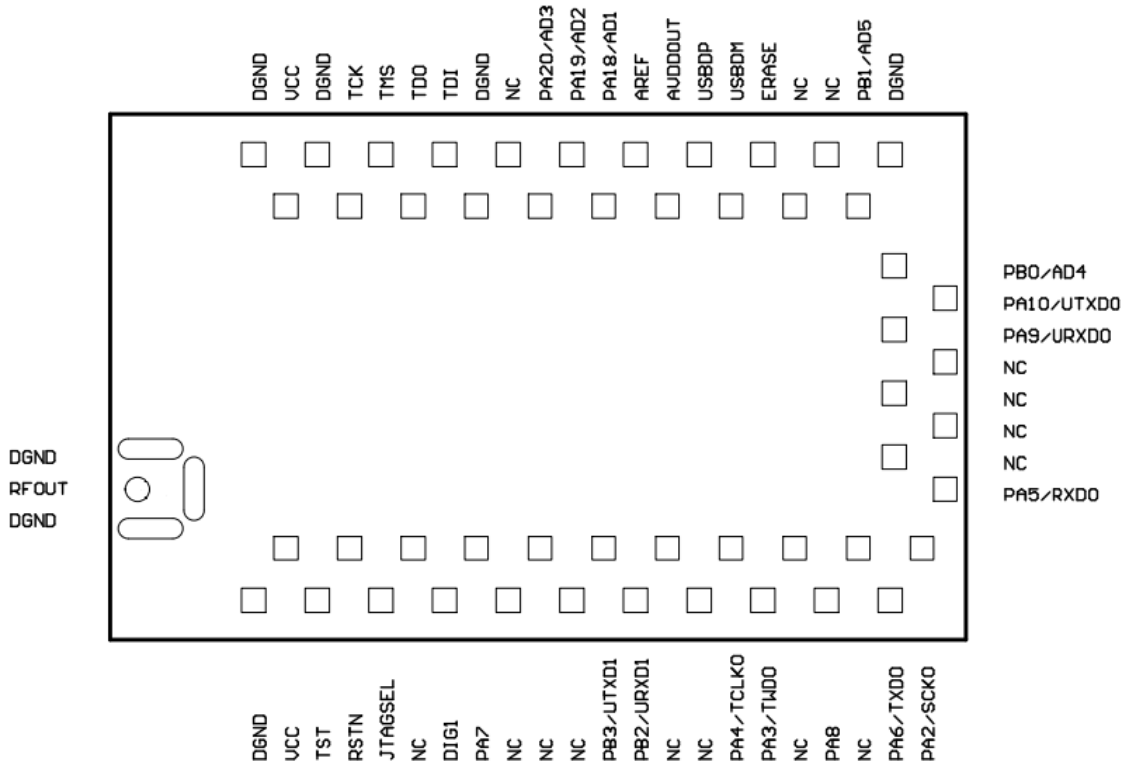


Figure 24: Pad numbering and signal names of deRFsam3-23M10-2 (top view)

Table 16: Description of available LGA pads and I/O port pins for deRFsam3-23M10-2

Description of available I/O port pins on header pins							
LGA Pad	*MCU Pin*	*TRX Pin*	*I/O port pin*	*Alternate function (signal name)*			*Comments*
1	-	-	GND				
2	-	-	VCC				1.8 V to 3.6 V
3	30	-	TST				**Must be connected to GND!**
4	29	-	RSTN				Reset
5	38	-	JTAGSEL				
6	-	-	NC				Leave unconnected
7	-	9	DIG1				Transceiver output pin
8	24	-	PA7	RTS0	PWMH3	XIN32	
9	-	-	NC				Leave unconnected
10	-	-	NC				Leave unconnected
11	-	-	NC				Leave unconnected
12	6	-	PB3	UTXD1	PCK2	AD7	UART1
13	5	-	PB2	URXD1	NPCS2	AD6	UART1
14	-	-	NC				Leave unconnected
15	-	-	NC				Leave unconnected
16	28	-	PA4	TWCK0	TCLK0		TWI
17	31	-	PA3	TWD0	NPCS3		TWI
18	-	-	NC				Leave unconnected
19	23	-	PA8	CTS0		XOUT32	
20	-	-	NC				Leave unconnected
21	26	-	PA6	TXD0	PCK0		USART0
22	32	-	PA2	SCK0	PWMH2		USART0
23	27	-	PA5	RXD0	NPCS3		
24	-	-	NC				Leave unconnected
25	-	-	NC				Leave unconnected
26	-	-	NC				Leave unconnected
27	-	-	NC				Leave unconnected
28	22	-	PA9	URXD0	NPCS1	PWMFI0	UART0
29	21	-	PA10	UTXD0	NPCS2		UART0
30	3	-	PB0		PWMH0	AD4	
31	-	-	GND				
32	4	-	PB1		PWM1	AD5	

33	-	-	NC				Leave unconnected
34	-	-	NC				Leave unconnected
35	42	-	PB12		PWML1	ERASE[4]	ERASE pin depending on program method necessary
36	43	-	PB10	DDM			Native USB
37	44	-	PB11	DDP			Native USB
38	29	-	AVDD				**Leave unconnected if unused (1.8V TRX Voltage Output)** Internal 1uF capacitor
39	1	-	AREF				No internal capacitor assembled
40	10	-	PA18		PCK2	AD1	
41	11	-	PA19		PWML0	AD2	
42	12	-	PA20		PWML1	AD3	
43	-	-	NC				Leave unconnected
44	-	-	GND				
45	25	-	PB4	TWD1	PWMH2	TDI	JTAG
46	37	-	PB5	TWCK1	PWML0	TDO	JTAG
47	39	-	PB6	SWDIO		TMS	JTAG
48	40	-	PB7	SWCLK		TCK	JTAG
49	-	-	GND				
50	-	-	VCC				1.8 V to 3.6 V
51	-	-	GND				

[4] See **Section** Fehler! Verweisquelle konnte nicht gefunden werden. for more information of the usage of ERASE pin

7.3. Signals of deRFsam3-23M10-3R

The radio module deRFsam3-23M10-3R has 55 LGA pads. The ‘1’ marking is shown in **Figure 26**. Consider that the pin numbering in **Figure 27** is shown from top view. All available LGA pads are listed in **Table 17**.

Figure 25: deRFsam3-23M10-3R (top view)

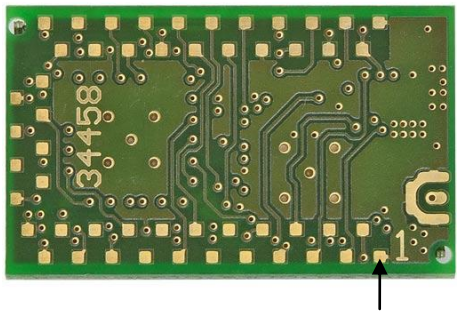


Figure 26: deRFsam3-23M10-3R (bottom view)

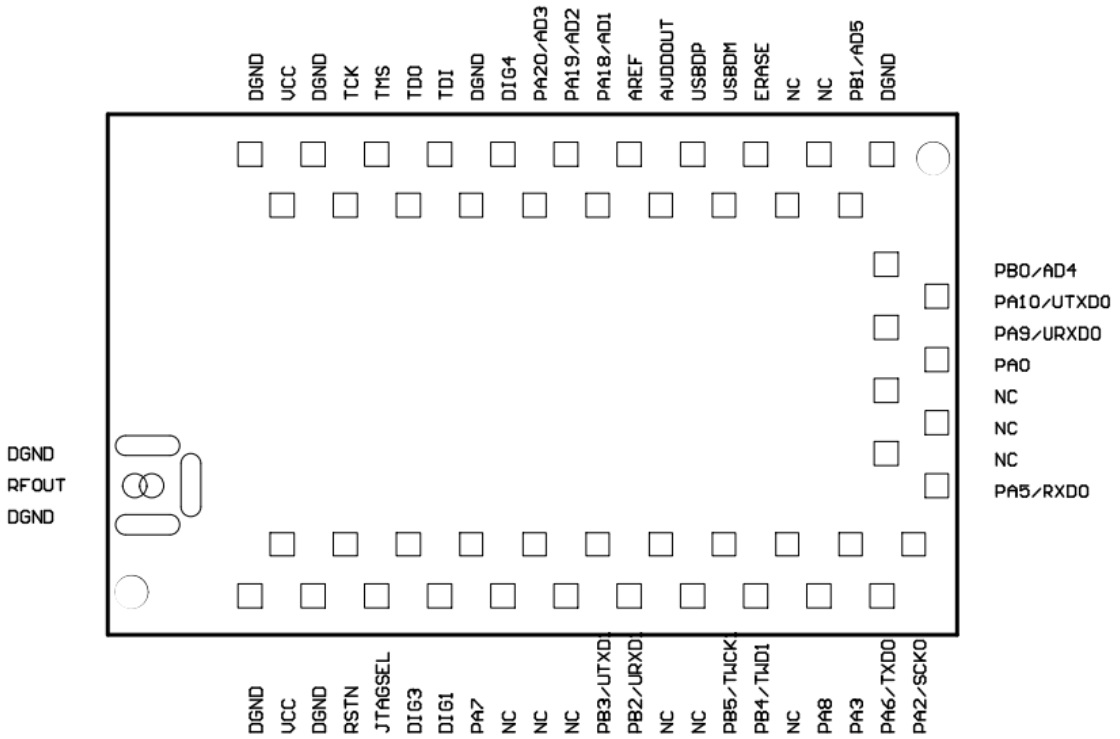


Figure 27: Pad numbering and signal names of deRFsam3-23M10-3R (top view)

Table 17: Description of available LGA pads and I/O port pins for deRFsam3-23M10-3R

Description of available I/O port pins on header pins							
LGA Pad	*MCU Pin*	*TRX Pin*	*I/O port pin*	*Alternate function (signal name)*			*Comments*
1	-	-	GND				
2	-	-	VCC				1.8 V to 3.6 V
3	30	-	TST				**Must be connected to GND!**
4	29	-	RSTN				Reset
5	38	-	JTAGSEL				
6	-	1	DIG3				Transceiver output pin
7	-	9	DIG1				Transceiver output pin
8	24	-	PA7	RTS0	PWMH3	XIN32	
9	-	-	NC				Leave unconnected
10	-	-	NC				Leave unconnected
11	-	-	NC				Leave unconnected
12	6	-	PB3	UTXD1	PCK2	AD7	UART1
13	5	-	PB2	URXD1	NPCS2	AD6	UART1
14	-	-	NC				Leave unconnected
15	-	-	NC				Leave unconnected
16	28	-	PB5	TWCK1	PWML0	TDO	TWI[7]
17	31	-	PB4	TWD1	PWMH2	TDI	TWI[6]
18	-	-	NC				Leave unconnected
19	23	-	PA8	CTS0		XOUT32	
20	-	-	PA3	TWD0	NPCS3		
21	26	-	PA6	TXD0	PCK0		USART0
22	32	-	PA2	SCK0	PWMH2		USART0
23	27	-	PA5	RXD0	NPCS3		USART0
24	-	-	NC				Leave unconnected
25	-	-	NC				Leave unconnected
26	-	-	NC				Leave unconnected
27	-	-	PA0	TIOA0	PWMH0		
28	22	-	PA9	URXD0	NPCS1	PWMFI0	UART0
29	21	-	PA10	UTXD0	NPCS2		UART0
30	3	-	PB0		PWMH0	AD4	
31	-	-	GND				
32	4	-	PB1		PWM1	AD5	

33	-	-	NC				Leave unconnected
34	-	-	NC				Leave unconnected
35	42	-	PB12		PWML1	ERASE[5]	ERASE pin depending on program method necessary
36	43	-	PB10	DDM			Native USB
37	44	-	PB11	DDP			Native USB
38	29	-	AVDD				**Leave unconnected if unused (1.8 V TRX Voltage Output)** Internal 1 uF capacitor
39	1	-	AREF				No internal capacitor assembled
40	10	-	PA18		PCK2	AD1	
41	11	-	PA19		PWML0	AD2	
42	12	-	PA20		PWML1	AD3	
43	-	2	DIG4				Transceiver output pin
44	-	-	GND				
45	25	-	PB4	TWD1	PWMH2	TDI	JTAG[6]
46	37	-	PB5	TWCK1	PWML0	TDO	JTAG[7]
47	39	-	PB6	SWDIO		TMS	JTAG
48	40	-	PB7	SWCLK		TCK	JTAG
49	-	-	GND				
50	-	-	VCC				1.8 V to 3.6 V
51	-	-	GND				

[5] See **Section** Fehler! Verweisquelle konnte nicht gefunden werden. for more information of the usage of ERASE pin

[6] Signal PB4 has the double functionality as ‘JTAG TDI’ and ‘TWI Data 1’. It is available on LGA pad 17 and 45. JTAG is the default function after reset. If TWI function is required, the JTAG interface must be deactivated in the MCU matrix register **[5]**. After that the two-wire interface can be initialized. In this case, programming is not possible until the JTAG pin functionality is reconfigured.

[7] Signal PB5 has the double functionality as ‘JTAG TDO’ and ‘TWI Clock 1’. It is available on LGA pad 16 and 46. JTAG is the default function after reset. If TWI function is required, the JTAG interface must be deactivated in the MCU matrix register **[5]**. After that the two-wire interface can be initialized. In this case, programming is not possible until the JTAG pin functionality is reconfigured.

7.4. Internal MCU to transceiver connection

The onboard transceiver is controlled by SPI (MOSI, MISO, SPCK) of the microcontroller. Additionally, other signals are available: IRQ, CLKM, RXTS, SELN, RST, SLPTR. A detailed description of their functionality can be found on transceiver datasheets **[2]**, **[3]** and **[4]**.

Table 18: Transceiver control signals

Transceiver control signals					
LGA Pad	*MCU Pin*	*TRX Pin*	*I/O port pin*	*Transceiver function (signal name)*	*Comments*
-	35	24	PA1	IRQ	1. Interrupt request signal 2. Buffer-level mode indicator
-	36	17	PA0[8]	CLKM	Master clock signal output
			PA4[9]		
-	15	10	PA15	RXTS	1. Inverted DIG1 2. Signal IRQ_2 (RX_START) for RX Frame Time Stamping
-	16	19	PA14	SCK	SPI Clock
-	17	22	PA13	MOSI	SPI data input
-	19	20	PA12	MISO	SPI data output
-	20	23	PA11	SELN	SPI select
-	14	8	PA16	RST	Chip reset, active low
	9	11	PA17	SLPTR	Control sleep, transmit start, and receive states

[8] CLKM connected with port PA0 on radio modules deRFsam3-13M10 and deRFsam3-23M10-2.

[9] CLKM connected with port PA4 is only valid for deRFsam3-23M10-3R.

7.5. External front-end and antenna diversity control

The deRFsam3-13M10 and deRFsam3-23M10-3R radio modules offer the feature to control external front-end components and to support antenna diversity. Though, the radio module deRFsam3-23M10-2 supports only antenna diversity. **Table 19** and **Table 20** show the logic values of the control signals. A logic '0' is specified with a voltage level of 0 to 0.3 V. A logic '1' is specified with a value of VCC - 0.3 V to 3.6 V.

An application circuit is shown in **Section 10.5**.

Antenna Diversity

The antenna diversity algorithm is enabled with setting bit ANT_EXT_SW_EN=1 in the transceiver register ANT_DIV. In this case the internal connection of control pins DIG1 and DIG2 to digital ground is disabled. They provide a differential control signal to the RF antenna switch. Please refer to transceiver datasheets **[2]**, **[3]** and **[4]** for detailed register settings.

Table 19: antenna diversity control

Mode description	DIG1	DIG2
TRX off Sleep mode	Disable register bit ANT_EXT_SW_EN to reduce the power consumption of external RF switch.	
ANT0	0	1
ANT1	1	0

Front end

The control of front-end components can be realized with the signals DIG3 and DIG4. The function will be enabled with bit PA_EXT_EN of register TRX_CTRL_1 which configure both pins as outputs. While transmission is turned off DIG3 is set to '0' and DIG4 is set to '1'. When the transceiver starts transmission the polarity will be changed. Both pins can be used to control PA, LNA and RF switches. Please refer to transceiver datasheets **[2]** and **[4]** for detailed register settings.

Table 20: front-end control

Mode description	PG0/DIG3	PF3/DIG4
TRX off Sleep mode	Disable register bit PA_EXT_EN to reduce the power consumption of external front-end devices.	
TRX off	0	1
TRX on	1	0

Sleep mode

To optimize the power consumption of external front-end components, it is useful to use a dedicated GPIO to set the PA into sleep mode, if applicable or to switch an additionally MOSFET, which supplies the PA.

7.6. Signal description

The available signals are described in **Table 21**. Please refer to **[5]** for more information of all dedicated signals.

Table 21: Signal description list

Signal name	Function	Type	Active Level	Comments
Power				
VCC	Voltage Regulator Power Supply Input	Power		
GND		Ground		
Clocks and Oscillators				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PCK0 – PCK2	Programmable Clock Output	Output		
JTAG				
TCK	Test Clock	Input		No pull-up resistor on module
TDI	Test Data In	Input		No pull-up resistor on module
TDO	Test Data Out	Output		
TDM	Test Mode Select	Input		No pull-up resistor on module
JTAGSEL	JTAG Selection	Input		Permanent internal pull-down
Flash Memory				
ERASE[10]	Flash and NVM Configuration Bits Erase Command	Input		
Reset				
RSTN	Microcontroller Reset	I/O	Low	Pull-up resistor[11]
TST	Test Select	Input		Permanent Internal pull-down
UART				
UTXD0 UTXD1	Transmit Data			
URXD0 URXD1	Receive Data			

[10] NVRAM with stored MAC address will be deleted if ERASE pin is used (see **Section 12.1**)

[11] Internal MCU pull-up resistor

USART				
SCK0	USARTx Serial Clock	I/O		
TXD0	USARTx Transmit Data	I/O		
RXD0	USARTx Receive Data	Input		
RTS0	USARTx Request To Send	Output		
CTS0	USARTx Clear To Send	Input		
Timer/Counter and PWM Controller				
TCLK0	TC Channel 0 External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
PWMHx	PWM Waveform Output High for channel x	Output		
PWMLx	PWM Waveform Output Low for channel x	Output		
PWMFI0	PWM Fault Input	Input		
SPI				
MISO	SPI Master In/Slave Out	I/O		
MOSI	SPI Master Out/Slave In	I/O		
SCK	SPI Bus Serial Clock	I/O		
Two-Wire Interface				
TWD1	Two-Wire Serial Interface 1 Data	I/O		No pull-up resistor[12]
TWCK1	Two-Wire Serial Interface 1 Clock	I/O		No pull-up resistor[12]
Analog-to-Digital Converter				
ADC0 - ADC7	Analog Inputs	Analog		
AREF	Analog Reference	Analog		
AVDDOUT	1.8 V Regulated Analog Supply Voltage Output from Transceiver	Analog		
USB Full Speed Device				
DDM	USB Full Speed Data -	Analog		
DDP	USB Full Speed Data +	Analog		

[12] External 4k7 pull-up resistors necessary for proper two-wire interface functionality

8. PCB design

The PCB design of a radio module base board is important for a proper performance of peripherals and the radio. The next subsections give design hints to create a custom base board. The adapter boards shown in **section 14** are well reference design starting points for custom specific boards. Please contact the dresden elektronik support team for adapter board design files.

8.1. Technology

The described design has the main goal to use standard PCB technology to reduce the costs and cover a wider application range.

Design parameters

- 150 µm manufacturing process
- 4 layer PCB with FR4 prepregs
- No via plugging
- Via hole size = 0.2 mm
- Via diameter = 0.6 mm

8.2. Base board footprint

The footprint for a custom base board depends on the used radio module. The mechanical dimensions are shown in **Section 5**. The following part describes an example to design a base board.

Properties of stencil and solder paste

- Stencil = 130 µm thickness
- Lead free solder paste (particle size from 20 to 38 µm)

Properties of signal pads

- Signal pad dimension = 0.6 x 0.6 mm (rectangular, red)
- Signal pad cut-out on stencil = 0.6 x 0.6 mm (rectangular, grey)
- Clearance to solder stop = 0.1 mm (purple)

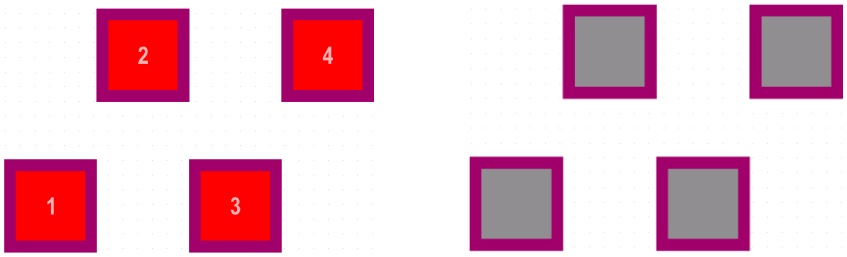


Figure 28: signal pad footprint design

Properties of RF pads

- RF ground pad dimension = 1.6 x 0.5 mm (round, red)
- RF ground pad cut-out on stencil = 1.3 x 0.2 mm (round, grey)
- RF signal-out pad dimension = 0.6 x 0.6 mm (round, red)

- RF signal-out pad cut-out on stencil = 0.6 x 0.6 mm (round, grey)
- Clearance to solder stop = 0.1 mm (purple)

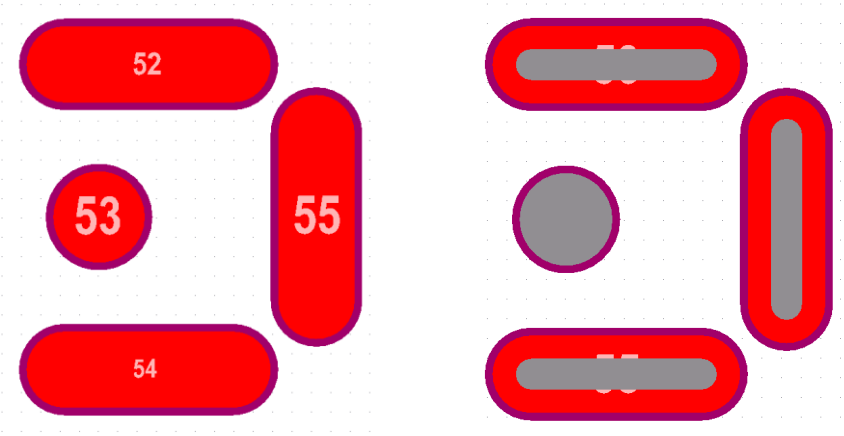


Figure 29: RF pad footprint design (top view)

8.2.1. Footprint of deRFsam3 radio modules

The exemplary base board footprint for deRFsam3 radio modules is shown in **Figure 30**. The top layer (red) is visible, the mid and bottom layer(s) are hidden. The rectangular signal pad copper area (red, not visible) and the paste dimension (grey) have the same size of 0.6 x 0.6 mm. The solder stop clearance (purple) has a value of 0.1 mm.

The RF ground pads are connected to each other and to the board ground to ensure a proper ground area. The RF ground area in **Figure 30** has a vertical dimension of 4.1 mm. The ground vias are not plugged. In this area are no other radio module signals. An unintentional short-circuit is therefore accepted. Do not place copper on any other area among the entire module. Solder stop could be used everywhere.

The RF trace design depends on the used base board and is described detailed in **Section 8.5**.

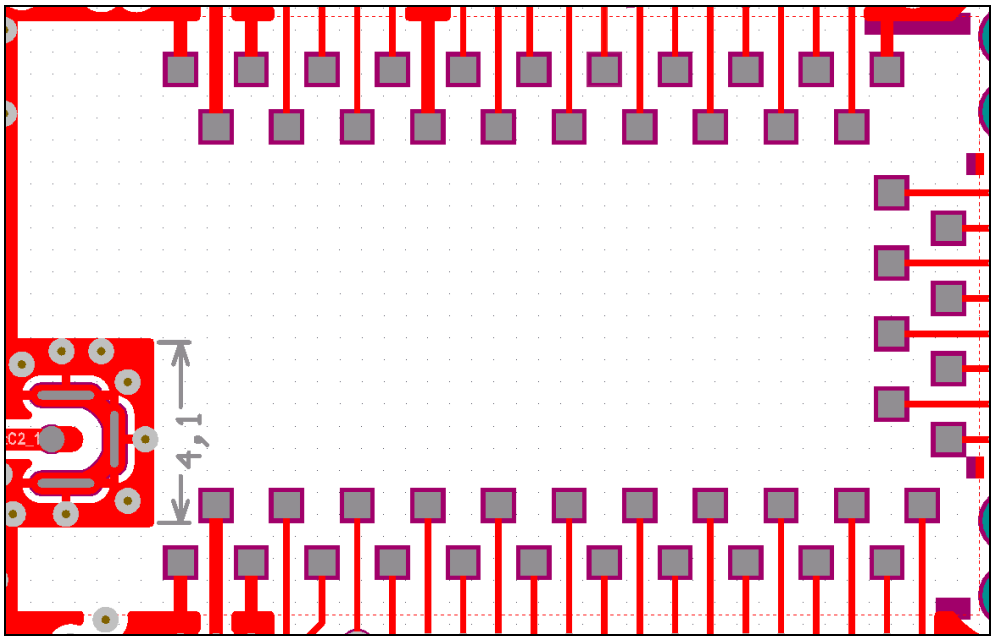


Figure 30: Exemplary base board footprint for deRFsam3-23M10-2 (top view)

8.3. Ground plane

The performance of RF applications mainly depends on the ground plane design. The often used chip ceramic antennas are very tiny, but they need a proper ground plane to establish a good radiation pattern. Every board design is different and cannot easily be compared to each other. Some practical notes for the ground plane design are described below:

- Regard the design guideline of the antenna manufacturer
- Use closed ground planes on the PCB edges on top and bottom layer
- Connect the ground planes with a lot of vias. Place it inside the PCB like a chessboard and on the edges very closely.

8.4. Layers

The use of 2 or 4 layer boards have advantages and disadvantages for the design of a custom base board.

Table 22: 2 and 4 layer board properties in comparison

2 layer board	4 layer board
(-) only 2 layers available for routing the traces and design a proper ground area	**(+)** 4 layers available for routing the traces and design a proper ground area
(-) only 1 layer available for routing the traces under the module	**(+)** 3 layers available for routing the traces under the module
(-) no separate VCC plane usable	**(+)** separate VCC plane usable
(+) cheaper than 4 layers	**(-)** more expensive than 2 layers

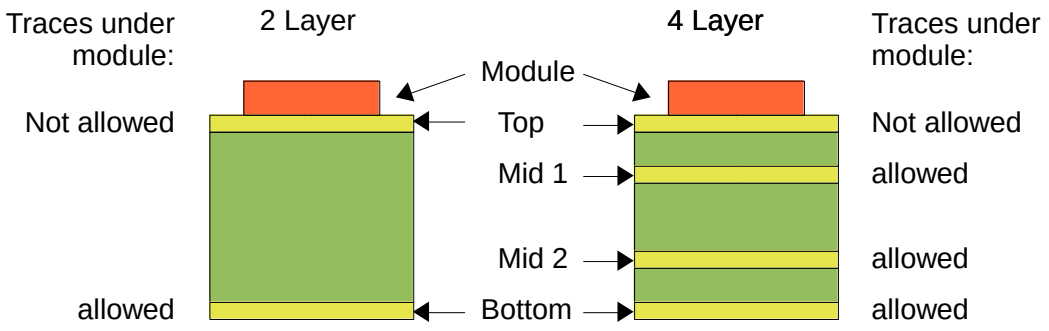


Figure 31: Comparison between 2 and 4 layer boards

8.5. Traces

Common signal traces should be designed with these guidelines:

- Traces on top layer are not allowed under the module (see **Figure 31**)
- Traces on mid layers and Bottom layers are allowed (see **Figure 31**)
- Route traces straight away from module (see **Figure 30**)
- Do not use heat traps of components directly on the RF trace
- Do not use 90 degree corners. Better is 45 degree or rounded corners.

The trace design for RF signals has a lot of more important points to regard. It defines the trace impedance and therefore the signal reflection and transmission. The most commonly used RF trace designs are Microstrip and Grounded Coplanar Wave Guide (GCPW). The dimension of the trace is depending on the used PCB material, the height of the material to the next ground plane, a PCB with or without a ground plane, the trace width and for GCPW the gap to the top ground plane. The calculation is not trivial, therefore specific literature and web content is available (see **[1]**).

The reference plane to the GCPW should always be a ground area, that means the bottom layer for a 2 layer design and mid layer 1 for a 4 layer design (see **Figure 32**). Furthermore, it is important to use a PCB material with a known layer stack and relative permittivity. Small differences in the material thickness have a great influence on the trace impedance, especially on 4 layer designs.

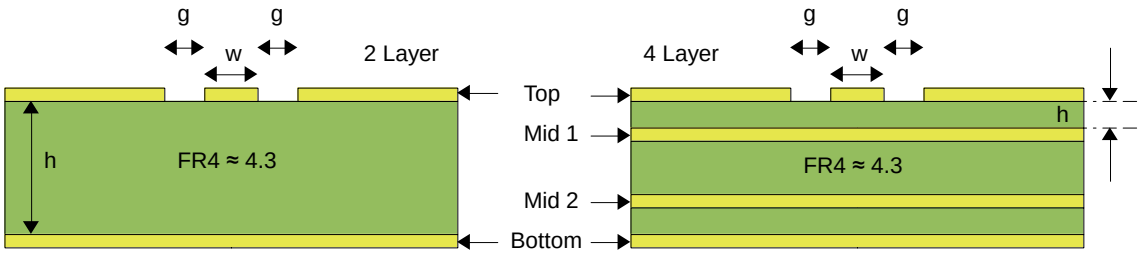


Figure 32: GCPW trace design

8.6. Placement on PCB

The PCB design of the radio module base board and placement affects the radio characteristic. The radio modules with RF pads could be placed everywhere on the PCB. But it should be enough space for routing a RF trace to a coaxial connector or to an onboard antenna. The chip antenna should be placed at the edge or side of a base board. Please refer to manufacturer's datasheet for recommended placement and ground plane clearance.

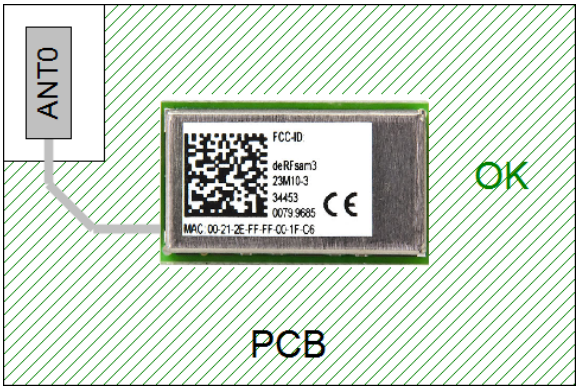


Figure 33: Placing the radio module and antenna

Do not place ground areas below the radio module (see **Section 8.4**) and near the chip-antenna.

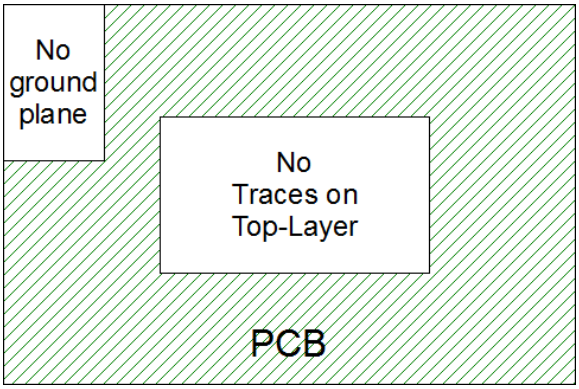


Figure 34: No ground plane and traces

8.7. Fiducial marker

Usually the radio module will be placed with a SMT placement system. The pick-and-place machine uses an internal camera system to match the pick-and-place data with the PCB to ensure that all components are placed correctly. The component orientation is realized with fiducial markers on the PCB. Mostly used are round markers without solder mask and solder paste (see black arrows in **Figure 35**). It is sufficient to place three round markers at different corners of the PCB to ensure a proper placement of common SMT components like resistors, capacitor or diodes and transistors. Big sized components with bottom pins like BGA or LGA should have their own fiducial markers to avoid placement errors in the assembly process. We propose a minimum of two diagonal edge markers without solder mask and paste, better a marker on each corner of the radio module (see red arrows in **Figure 35**).

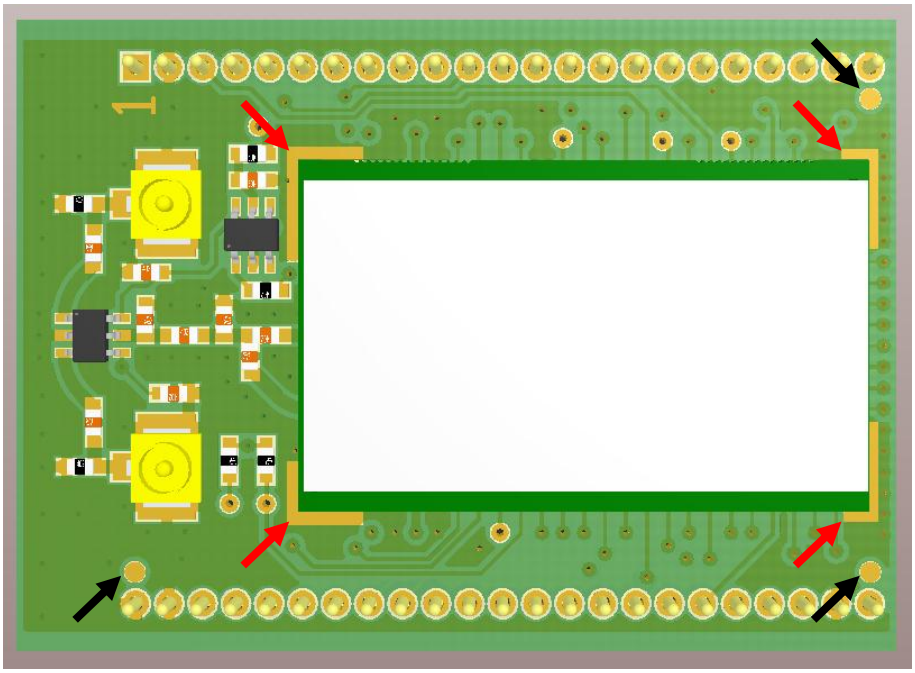


Figure 35: Fiducial markers on a radio module base board

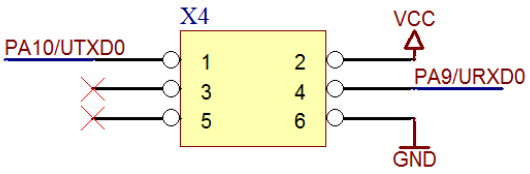
9. Clock

The radio module contains an onboard 18.432 MHz 30 ppm quartz crystal for the MCU and a 16.000 MHz 10 ppm quartz crystal for the onboard transceiver. For optimum RF timing characteristics it is necessary to use a low tolerance crystal.

10. Application circuits

10.1. UART

Two UART and one USART interfaces are available on the radio modules. For communication to a host with a different supply voltage domain it is necessary to use a level shifter. We recommend the USB level shifter by dresden elektronik for usage with a USB host. The level shifter can be connected to the custom base board via 100 mil 2x3 pin header. The pin assignment should be designed as below in **Figure 36**. For an UART connection it is sufficient to use only TXD, RXD and GROUND signals.

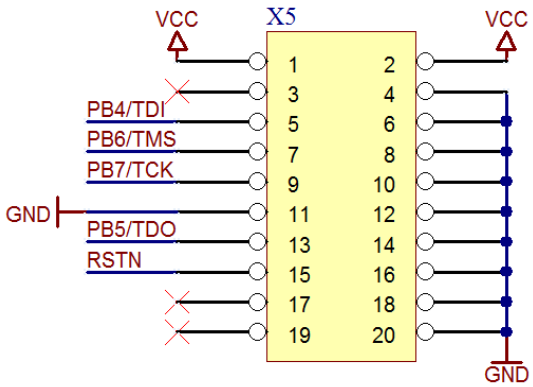


1. PE1/TXD0
2. VCC
3. Not connected
4. PE0/RXD0
5. Not connected
6. GND

Figure 36: 100 mil 2x3 pin header for UART0

10.2. JTAG

The ARM based radio modules can be programmed via JTAG interface. For JTAG connection a 100 mil 2x5 pin header should be used. The pin assignment is given in **Figure 37**. We recommend the use of 'Atmel SAM-ICE' programmer.



1. VCC	11. GND
2. VCC	12. GND
3. nTRST	13. TDO
4. GND	14. GND
5. TDI	15. RSTN
6. GND	16. GND
7. TMS	17. NC
8. GND	18. GND
9. TCK	19. NC
10. GND	20. GND

Figure 37: 100 mil 2x5 pin header for JTAG

10.3. TWI

The connection of external peripherals or sensors via two-wire interface is possible by using the TWI clock signal PA4/TWCK0 and TWI data signal PA3/TWD0. The necessary pull-up resistors must be placed externally on the base board. We recommend the use of 4.7 kΩ resistors as shown in **Figure 38**.

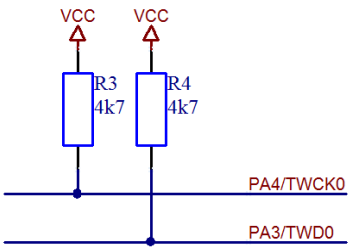


Figure 38: Two-wire interface

10.4. USB

The deRFsam3 radio modules have an internal native USB device transceiver. The USB pins are shared with I/O lines. By default, the USB function is activated. Only some external components are necessary to use the USB function (see **Figure 39**).

Necessary

- R5 and R6 are termination resistors (27 ohms).
- A suitable USB socket (type A for USB host and type B for USB device).

Recommended

- Capacitors C1 and C2 (15 pF) build a low-pass with the termination resistors.
- Diode array D1 protects the radio module against over or under voltage events on USB voltage supply line and differential signal lines.

Optional

- Resistors R7 (47 kOhm) and R8 (27 kOhm) connected from USB supply voltage to an I/O port are useful to detect all device states.

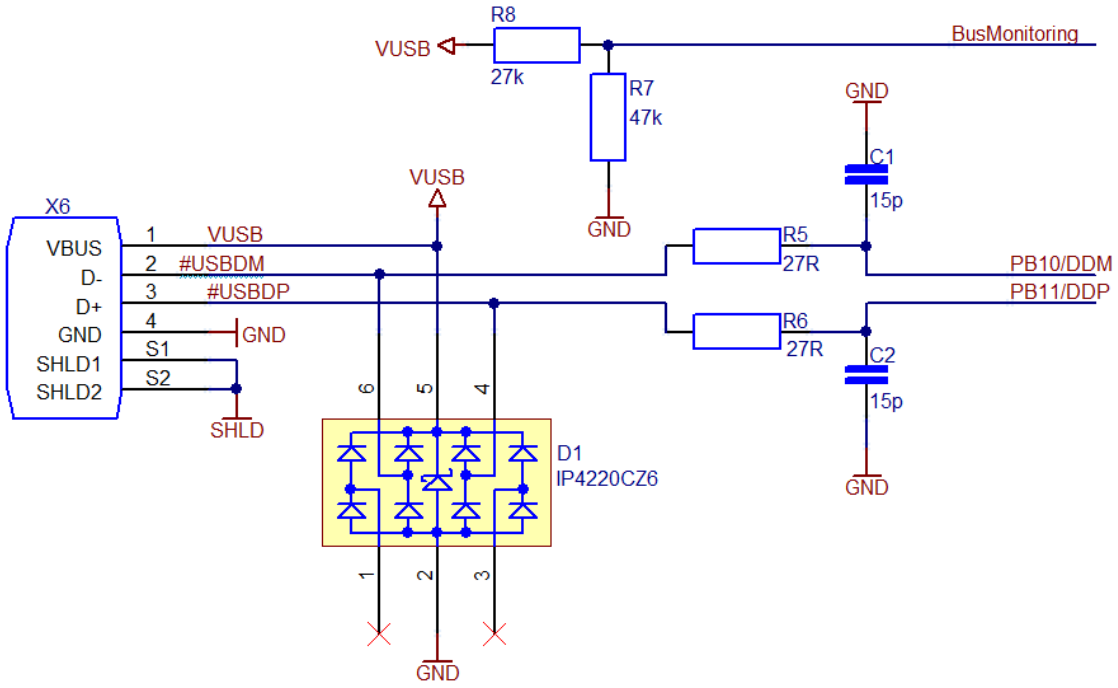


Figure 39: USB interface

10.5. External front end and antenna diversity

The radio module deRFsam3-13M10 and 23M10-3R can be connected with an external front end including power amplifier (PA) for transmission and low noise block (LNA) for receiving. **Figure 40** shows a possible design as block diagram. A custom design can contain a single PA or single LNA or a complete integrated front-end chip. It depends mainly on the application. Furthermore, it is possible to include a RF switch for driving the antenna diversity feature.

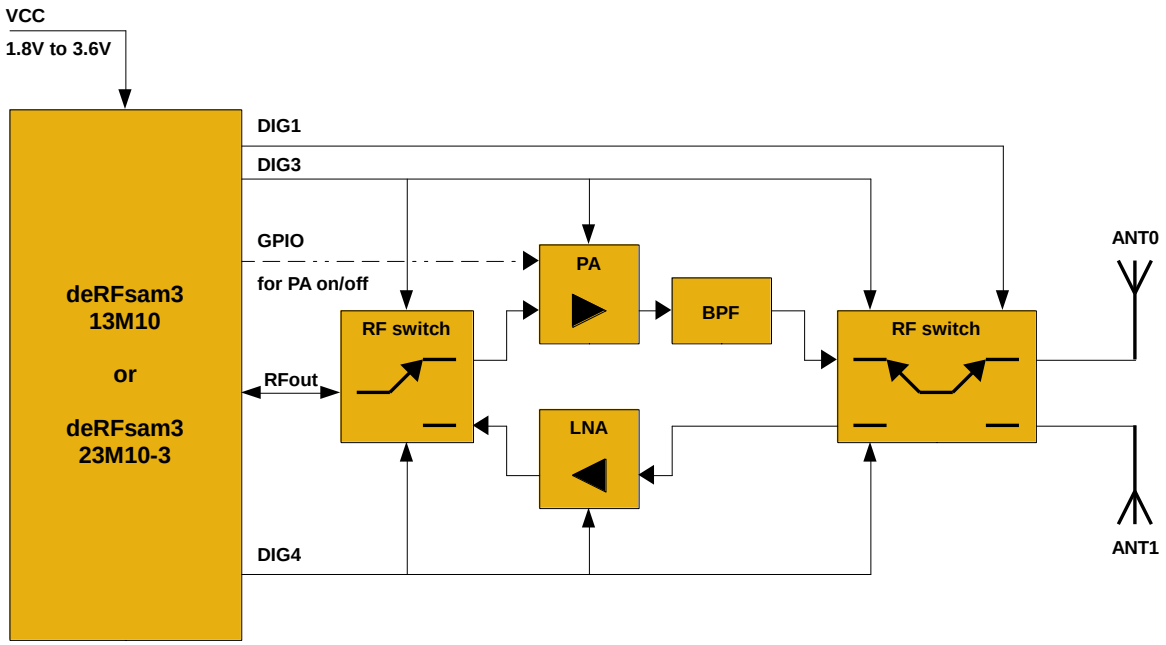


Figure 40: block diagram for external PA/LNA and antenna diversity control

Unbalanced RF output

The deRFsam3 radio module has a 50 Ω unbalanced RF output. For designs with external RF power amplifier a RF switch is required to separate the TX and RX path.

RF switches to PA, LNA and antenna

The switch must have 50 Ω inputs and outputs for the RF signal. The switch control could be realized with the DIG3 and DIG4 signal of the radio module. Refer to **Section 7.5** for detailed information.

PA

The PA has to be placed in the TX path after the RF switch. It is important to regard the PA's manufacturer datasheet and application notes, especially for designing the power supply and ground areas. A poor design could cause a very poor RF performance. For energy efficiency it is useful to activate the PA only during TX signal transmission. In this case the DIG3 signal can be used as switch for (de-)activating the PA. Some PAs have the possibility to set them into sleep state. This application can be realized via dedicated GPIO pin. Refer to **Section 7.5** for more information.

BPF
The use of a band-pass filter is optional. It depends on the PA properties. Some PAs have an internal BPF and other have none. The BPF is necessary to suppress spurious emissions of the harmonics and to be compliant with national EMI limits. It is possible to use an integrated BPF part or discrete parts. The advantage of the first variant is that the BPF characteristic is known and published in the manufacturer's datasheet.

LNA
The LNA could be used to amplify the received signal. Please regard the manufacturer's datasheet for a proper design. The control could be done by DIG4 signal. Refer to **Section 7.5** for more information.

RF switch for antenna diversity
The switch must have 50 Ω inputs and outputs for the RF signal. It is possible to use a separate switch with 2 inputs and 2 outputs or use another (third) switch following the switch required for the PA/LNA. Antenna diversity switching could be controlled via DIG1. Refer to **Section 7.5** for more information.

Certification
The customer has to ensure, that custom front-end and antenna diversity designs based on the radio module deRFsam3-13M10 or deRFsam3-23M10-3R will meet all national regulatory requirements of the assignment location and to have all necessary certifications, device registration or identification numbers.

11. Positioning feature

The deRFsam3-23M10-3R radio module features the functionality of ranging and can therefore be used for advanced localization solutions. Ranging means to determine the distance of a target device compared to an anchor device. The ranging feature uses phase delay measurements by exploiting the ranging partner as an active reflector. This enables far better results than receive signal strength based ranging.

The localization of a target is calculated from the measured distances with appropriate localization algorithms resulting in coordinates in the x-, y- and z-plane. However, the localization algorithms are not part of the ranging features of the deRFsam3-23M10-3R radio module.

Detailed information and support about the ranging functionalities is available from our partner **ZIGPOS.** A corresponding evaluation kit powered by **ZIGPOS** is available in our webshop.

12. Programming

The programming procedures are described in the documentation **[6]**, which is available as PDF document on the dresden elektronik webpage. It describes step-by-step the update process of the radio module, the required software and hardware for programming via JTAG and the driver installation on different operating systems.

12.1. ERASE pin

The ERASE pin on LGA pad '35' is used to reinitialize the flash content to an erased state. All firmware data and the saved MAC Address will be deleted! For normal operations, this pin can be left unconnected. The pin must be tied high (logic 1) for more than 220 ms to perform a flash erase operation.

13. Pre-flashed firmware

Actually, the radio modules will be delivered without pre-flashed firmware.

14. Adapter boards

dresden elektronik offers these radio modules soldered on suitable adapter boards. These boards can be plugged into dresden elektronik's development hardware platforms deRFbreakout Board, deRFnode or deRFgateway. For detailed information please refer to the respective adapter board datasheets **[7], [8]**.

Figure 41: deRFsam3-13T02 adapter board with radio module deRFsam3-13M10

Figure 42: deRFsam3-23T02-2 adapter board with radio module deRFsam3-23M10-2

Figure 43: deRFsam3-23T09-3 adapter board with radio module deRFsam3-23M10-3R

15. Radio certification

15.1. United States (FCC)

The deRFsam3-13M10, deRFsam3-23M10-2 and deRFsam3-23M10-3R complies with the requirements of FCC part 15. The certification process is pending.

15.2. European Union (ETSI)

The deRFsam3-13M10, deRFsam3-23M10-2 and deRFsam3-23M10-3R are conform for use in European Union countries.

If the deRFsam3-13M10, deRFsam3-23M10-2 and deRFsam3-23M10-3R modules are incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonized EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive.

The manufacturer must maintain a copy of the deRFsam3-13M10, deRFsam3-23M10-2 and deRFsam3-23M10-3R modules documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

The “CE“ marking must be affixed to a visible location on the OEM product. The CE mark shall consist of the initials "CE" taking the following form:

- If the CE marking is reduced or enlarged, the proportions given in the above graduated drawing must be respected.
- The CE marking must have a height of at least 5 mm except where this is not possible on account of the nature of the apparatus
- The CE marking must be affixed visibly, legibly, and indelibly.

More detailed information about CE marking requirements you can find at "DIRECTIVE 1999/5/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL" on 9 March 1999 at section 12.

15.3. Approved antennas

The deRFsam3-13M10, deRFsam3-23M10-2 and deRFsam3-23M10-3R will be tested with external antennas. The approved antenna list will be updated when the certification process is done.

16. Ordering information

The product name includes the following information:

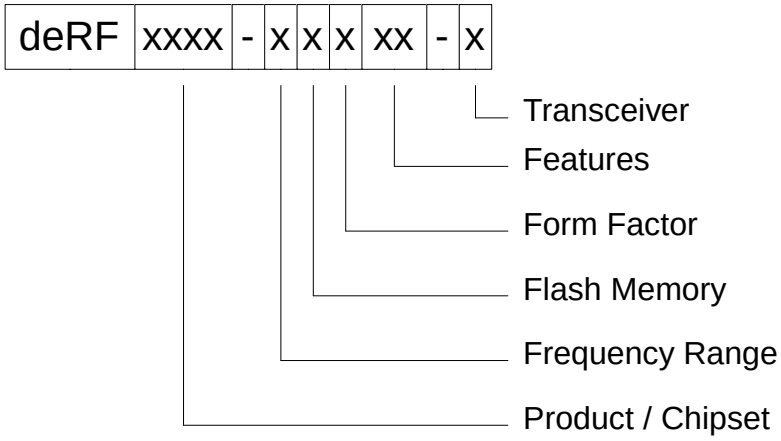


Table 23: Product name code

Product name code			
Information	*Code*	*Explanation*	*Comments*
Product / chipset	sam3		radio module
Frequency range	1	868.3 / 915 MHz	
	2	2.4 GHz	
Flash memory	3	256 kByte	
Size	M	OEM module	solderable
Features	10	RFOUT pad	
Transceiver (sub GHz)	empty	AT86RF212	
Transceiver (2.4 GHz)	2	AT86RF232	
	3R	AT86RF233	supports ranging

Table 24: Ordering information

Ordering information		
Part number	*Product name*	*Comments*
BN-034489	deRFsam3-13M10	solderable radio module with RFOUT pad, no pre-flashed firmware
BN-034490	deRFsam3-23M10-2	solderable radio module with RFOUT pad, no pre-flashed firmware
BN-600042	deRFsam3-23M10-3R	solderable radio module with RFOUT pad, no pre-flashed firmware

17. Packaging dimension

The radio modules will be delivered in a single packing (Tape & Reel on request).

18. Revision notes

Currently, no design issues of the radio modules are known.

All errata of the CORTEX-M3 MCU and transceivers are described in the datasheets **[2]**, **[3]**, **[4]** and **[5]**.

19. References

[1] Free RF&Microwave design software ‘AppCAD Version 3.0.2’ by Agilent Technologies; available on http://www.hp.woodshot.com/

[2] AT86RF212: Low Power 700/800/900 MHz Transceiver for IEEE802.15.4, ZigBee, 6LowPan, and ISM Applications; Datasheet; 8168C-MCU Wireless-02/10

[3] AT86RF232: Low Power 2.4 GHz Transceiver for IEEE802.15.4, ZigBee, 6LowPan, RF4CE and ISM Applications; Datasheet; 8321A-MCU Wireless-10/11

[4] AT86RF233: Low Power 2.4 GHz Transceiver for IEEE802.15.4, ZigBee, 6LowPan, RF4CE and ISM Applications; Datasheet; 8351B-MCU Wireless-06/12

[5] ATSAM3S4: AT91SAM ARM-based Flash MCU;
Datasheet; 6500D-ATARM-29/02/12

[6] User Manual Software Programming;
URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/oem-derfmega/description/?L=0&eID=dam_frontend_push&docID=1917

[7] Datasheet deRFsam3-13T02 | 23T02-2;
URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/adapter-boards-oem-modules/description/?L=1&eID=dam_frontend_push&docID=1821

[8] Datasheet deRFsam3-23T09-3;
URL: http://www.dresden-elektronik.de/funktechnik/service/downloads/documentation/?L=0&eID=dam_frontend_push&docID=2363

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